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An Agile Frequency Synthesizer/RF Generator for the SCAMP Terminal

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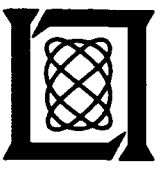

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This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

Gary Tutungian
Administrative Contracting Officer
Directorate of Contracted Support Management

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

AN AGILE FREQUENCY SYNTHESIZER/RF GENERATOR FOR THE SCAMP TERMINAL

H.M. WOLFSON
Group 66

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ABSTRACT

This report describes a combination agile synthesizer and reference frequency generator called the RF Generator, which was developed for use in the Advanced SCAMP (ASCAMP) program. The ASCAMP is a hand-carried, battery-powered, man-portable ground terminal that is being developed for EHF satellite communications. In order to successfully achieve a truly portable terminal, all of the subsystems and components in ASCAMP were designed with the following critical goals: low power, lightweight, and small size.

The RF Generator is based on a hybrid design approach of direct digital and direct analog synthesis techniques that was optimized for small size, low power consumption, fast tuning, low spurious, and low phase noise.

The RF Generator was conceived with the philosophy that simplicity of design would lead to a synthesizer that differentiates itself from those used in the past by its ease of fabrication and tuning. By avoiding more complex design approaches, namely, indirect analog (phase lock loops), a more easily produceable design could be achieved. An effort was made to minimize the amount of circuitry in the RF Generator, thereby making trade-offs in performance versus complexity and parts count when it was appropriate.

ACKNOWLEDGMENTS

The work presented in this paper was the result of several years of effort and was accomplished by a small group of dedicated people. I wish to thank John Murphy for his hard work and assistance throughout the entire development, assembly, testing, and debugging of the RF Generator; Larry Kushner for the design of the digital comb generator and valuable interchange and discussions during all phases of the development, from the initial architecture to final implementation; Dave Materna for the design and implementation of the hybrid SP6T switch and the switched filter bank, the TMXO Module, the 11-GHz filter, assistance with the DDS characterization and modeling, and many valuable discussions; Rick Magliocco and the Group 63 Hybrid Assembly Laboratory for assistance with the MIC designs and fabrication of all the high-frequency boards; Eileen Fox for mechanical packaging and design; Mark Moriarty for evaluation and layout of the DDS board; and George Gorski for his assistance and encouragement.

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1. INTRODUCTION

New synthesizer architectures [1] are required to meet the performance demands of modern spread spectrum, extremely high frequency (EHF) communications. The development of man-portable terminals imposes additional requirements on the electronics. These constraints can be summarized by the following points.

a. Small size, lightweight, and low dc power consumption

b. Broad bandwidth and high resolution

c. Extremely fast frequency switching and settling rates

d. Adequate spectral purity to prevent interference

The set of goals listed in item (a) are especially important for a man-portable terminal, while the last three goals are common to most EHF systems.

There are three basic approaches for designing a high-resolution frequency synthesizer that are commonly used: (a) indirect synthesis, which incorporates a voltage controlled oscillator (VCO) in a tunable phase lock loop (PLL); (b) direct analog synthesis, which incorporates cascaded stages of mix-and-divide networks to generate a desired resolution or number of channels; and (c) direct digital synthesis (DDS), which uses digital accumulators, a ROM, and a digital-to-analog converter (DAC). Many systems incorporate a mixture, or hybrid, of these designs in order to take advantage of the benefits of increased speed or improved resolution that one approach may have over another.

The synthesizer that is presented in this paper is a hybrid of direct digital and direct analog designs, which results in a unique frequency generator system ideally suited for a man-portable EHF terminal. This agile synthesizer has frequency settling times under 1 μs over a 600-MHz tuning range, which is centered at 11.1 GHz with 2.2-Hz resolution. Total noise power over a 10-MHz bandwidth, combining phase noise and spurious, is better than –30 dBc. The complete unit is less than 90 in^3, weighs 3.4 lb, and requires 17.5 W of dc power during continuous operation.

This report will describe some of the history of EHF synthesizers at Lincoln Laboratory, the philosophy and trade-offs that led to our design, design details and analyses of the frequency plan, spurious and phase noise, implementation details and the lessons learned, test techniques and measurement results, recommendations for future improvements, and conclusions.

2. HISTORY

This section will briefly discuss some background of the synthesizer systems that were developed at Lincoln Laboratory for use in MILSTAR ground terminals for the Army.

2.1 SCOTT TERMINAL

Between 1980 and 1985, Lincoln Laboratory developed an Advanced Development Model of the Army's SCOTT terminal. Three subsystems were required to provide frequency reference and hopping signals to the receiver and transmitter. These subsystems consisted of the Frequency Reference Unit, Frequency Synthesizer Unit, and the Upconverter Unit. The Frequency Synthesizer Unit weighed 65 lb, required 70 W of dc power, and had a total volume of 2000 in^3.

The synthesizer system provided full duplex operation via two independent synthesizers: one for the uplink and one for downlink. Each synthesizer (uplink and downlink) contained two phase lock loops (PLLs) whose rf outputs were multiplexed in a "ping-pong" manner. This system resulted in a fast hopping output for the receiver and transmitter. In other words, four PLL synthesizers were used to provide full duplex operation for the receiver and transmitter simultaneously.

2.2 SCAMP TERMINAL

Between 1983 and 1987, Lincoln Laboratory developed and built a new kind of MILSTAR terminal. The goal was a man-portable unit whose design focus was on a "minimal" system. Its purpose was to demonstrate the ability to communicate at EHF frequencies with the least amount of hardware possible. To attain the small size, weight, and power that a truly portable system would require, the terminal was designed to communicate using the standard EHF waveform, but only at half-duplex and at 75 bps.

The synthesizer system that was developed for SCAMP was based on a low-frequency DDS followed by a frequency multiplier chain (with a times-256 multiplication factor) to achieve the full bandwidth coverage at 11 GHz. This system had a very simple design that was acceptable for the SCAMP program and allowed the desired communication mode. The SCAMP RF Generator (RFG) had a volume of 140 in^3, weighed 4.5 lb, and required 12 W of dc power. It had a relatively high spurious and noise, so high that the transmitter carrier output would be suppressed by noise for some of the frequencies over its tuning range. Although based on a DDS, the SCAMP RFG had slow frequency settling that limited its utility to low hop rate communications, which was adequate for the SCAMP terminal.

For all of its limitations the SCAMP terminal and its synthesizer system was a valid proof of concept that a small and relatively noisy synthesizer was achievable and would yield acceptable performance for a MILSTAR terminal system. This achievement was proven by the many demonstrations of the SCAMP terminals in the field under many conditions such as operating in poor weather, operating indoors with the antenna aimed through windows, and operating in a battery-saving, low transmitter output power mode.

3. DESIGN GOALS

The design goals of the ASCAMP RF Generator (RFG) were based on the desired terminal performance. The ASCAMP terminal was designed to operate at all MILSTAR low data rates, yet be significantly smaller and lighter than the original SCAMP.

The RFG developed for ASCAMP was designed with performance goals similar to the SCOTT Advanced Development Model's synthesizer but with less weight, smaller size, and less dc power. The RFG had to change frequencies and settle in less than 1 μs. The ASCAMP requirement for the RFG's spectral purity was that less than 0.1 dB of the transmitter's output power be lost due to noise. The design goal for combined noise and spurious was that the RFG would meet the system needs of larger terminals.

In addition, the RFG for ASCAMP had to contain circuitry to provide reference frequencies for the receiver's downconversion stages and a reference clock for the digital subsystem. In other words, what was contained in the SCOTT's Frequency Synthesizer Unit, Frequency Reference Unit, and Upconverter Unit would all be provided by a single RFG that weighed 3.4 lb in 90 in^3. This unit would be smaller and lighter than the original SCAMP RFG, with the performance of the SCOTT synthesizer (in half-duplex mode).

4. POSSIBLE IMPLEMENTATION APPROACHES: ADVANTAGES AND DISADVANTAGES

There are three basic approaches for designing a high-resolution frequency synthesizer that are commonly used today: (a) indirect synthesis incorporating a voltage controlled oscillator (VCO) in a tunable phase lock loop (PLL); (b) direct analog synthesis, which incorporates cascaded stages of mix-and-divide networks to generate a desired resolution or number of channels; and (c) direct digital synthesis (DDS), which uses digital accumulators, a ROM look-up table, and a digital-to-analog converter (DAC). Many systems incorporate a hybrid of these designs in order to take advantage of increased speed or improved resolution that one approach may have over another.

4.1 INDIRECT SYNTHESIS

A simplified block diagram of a high-performance indirect/PLL synthesizer is shown in Figure 1. One of the primary disadvantages of PLLs is their relatively slow speed. A basic limitation of any PLL is that the tuning speed is proportional to the inverse of the closed loop bandwidth. A narrow loop bandwidth is required to keep the loop locked and to reduce phase noise, while a wide loop bandwidth is desired for fast tuning. To change output frequencies at the rate required for the EHF waveform, this class of synthesizer typically requires a significant amount of added circuitry [2]. A common solution to achieving the fast hopping requirement is to incorporate two independent PLLs whose outputs are time-multiplexed into the remaining rf hardware. The reason for this "ping-pong" arrangement is to ensure that each PLL has sufficient time to tune to a new frequency and settle before its output signal is used.

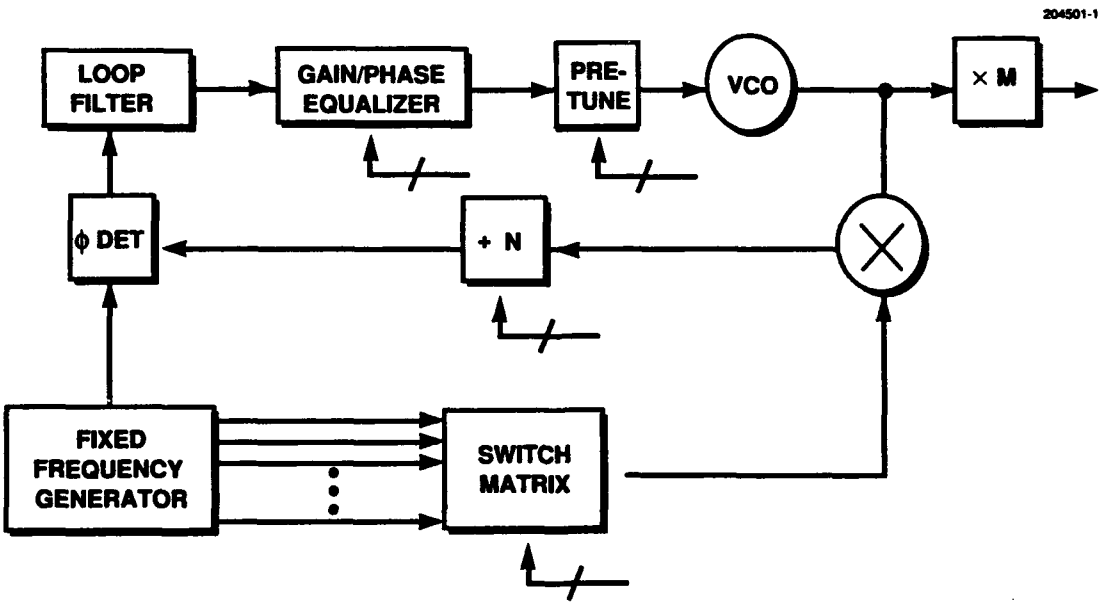


Figure 1. Simplified block diagram of indirect synthesizer.

Sometimes a PLL synthesizer may incorporate a DDS in its reference circuitry to increase resolution or to reduce its switching speed. A major drawback of this approach is that the PLL acts as a multiplier on any phase noise or spurious in its reference and that a DDS can have relatively high spurious. The resulting noise at the PLL output can seriously degrade system performance [2].

4.2 DIRECT ANALOG SYNTHESIS

Another common synthesizer design is the direct analog synthesizer. By cascading stages of multipliers, dividers, and mixers, a large number of separate frequencies or channels can be generated from a single reference (a simplified block diagram of the two stages of mix-and-divide is shown in Figure 2). The desired output signal can be rapidly switched between any set of frequencies at very fast speeds. The only speed limitations are the pin diode switches and the digital divider circuits, both of which can switch in under 1 μs. Many manufacturers of commercial test equipment use mix-and-divide designs for their synthesizers, and they report that excellent phase noise and spurious performance can be achieved with adequate physical and electrical isolation between the stages. The major drawbacks for this scheme are the sheer size and dc power that would be required to make a synthesizer of this type for our application. The frequency resolution that is required for the EHF waveform would require a very large number of cascaded mix-and-divide stages. Any practical implementation of direct analog synthesis would require a DDS (described below) as augmenting circuitry to provide the fine frequency resolution.

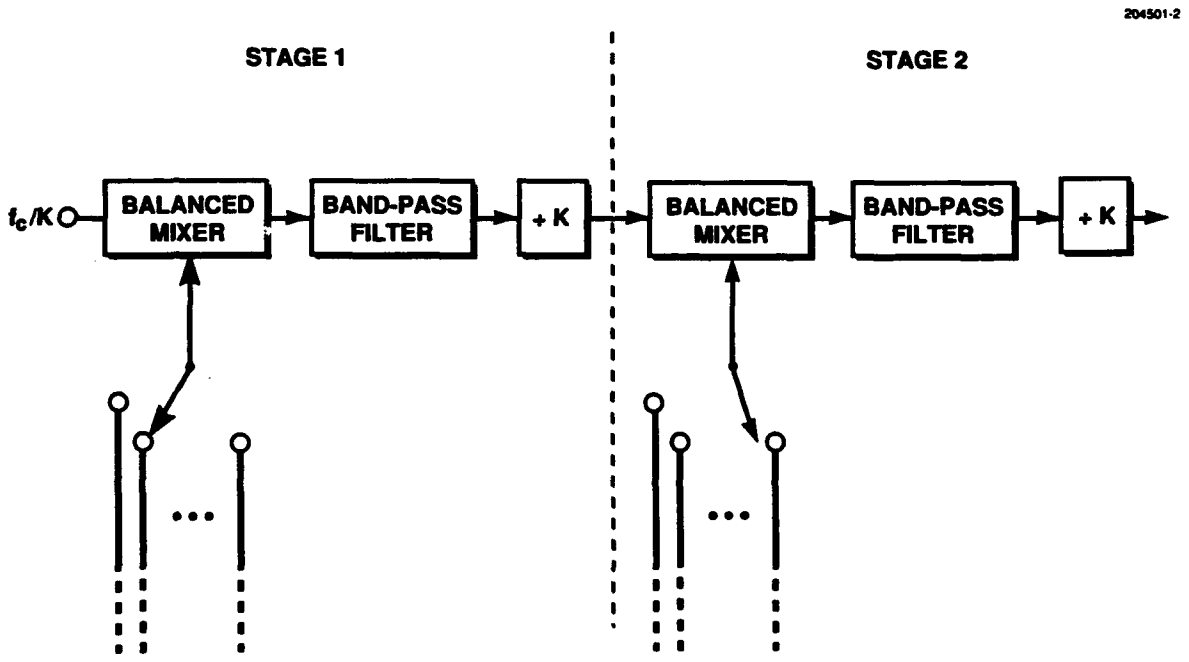


Figure 2. Block diagram of two stages of a mix-and-divide synthesizer.

4.3 DIRECT DIGITAL SYNTHESIS

The DDS synthesizer is a technology that was first developed in the 1970s [3]. A block diagram of a typical DDS is shown in Figure 3. The two major components of the DDS are a numerically controlled oscillator (NCO) [4] and a digital-to-analog converter (DAC). The NCO consists of an adder-register pair (also called a phase accumulator) and the ramp-to-sine-wave look-up ROM. The output of the DDS is related to the phase accumulator input by the following equation.

$$f_{out} = \frac{\text{Increment}}{2^N} * f_{clock} \quad , \tag{1}$$

where

f_{out}	is the output frequency of the DDS,
Increment	is the frequency command word input to the accumulator,
N	is the number of bits in the accumulator, and
f_{clock}	is the clocking frequency of the DDS.

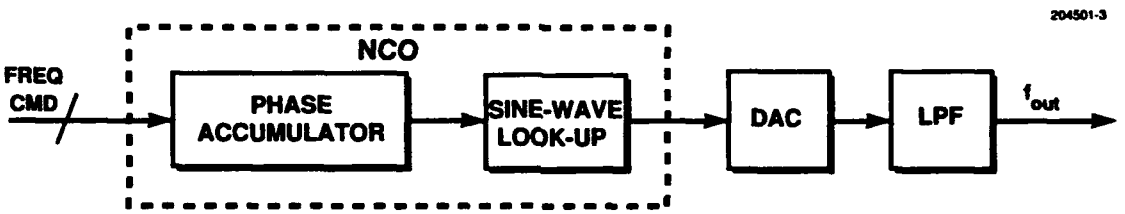


Figure 3. Direct digital synthesizer block diagram.

The DDS typically provides a low-frequency output with extremely high resolution and an excellent frequency switching speed. The resolution of a DDS can be made arbitrarily small with very little additional circuitry or added complexity. The switching time of a DDS is a function of the propagation delay through the digital gates and the settling time of the DAC and is typically within a few dozen clock cycles. Due to sampling theory, a DDS can only generate frequencies up to a maximum of one-half of the clock rate of the digital circuitry. Practically speaking, the maximum useful output of a DDS is limited in bandwidth to a range approximately between 10% and 40% of the clock rate. The high-frequency limitation is due to the anti-alias low-pass filter that must follow the DAC because all DDS synthesizers produce an alias term along with the desired output frequency.

$$f_{alias} = f_{clock} - f_{out} \quad . \tag{2}$$

The low-frequency limitation is due to the band-pass filter that is required after any upconversion (i.e., DDS frequencies near dc are difficult to process after an upconversion). These limitations of narrow bandwidth and low output frequency can be overcome with bandwidth expansion techniques described below.

The primary disadvantages of most DDSs are the unfortunate trade-offs between tuning frequency, dc power consumption, and spurious output. As described above, higher clock frequencies allow for higher output frequencies and broader tuning range. Most spurious from a DDS are caused by amplitude quantization, "glitch noise," and nonlinearities in the DAC. A very rough rule of thumb is that the spurious levels generated by a DAC quantization equals 6 dB times the number of input bits (e.g., an 8-bit DAC would have an ideal amplitude quantization spurious 48 dB lower than the carrier). However, as the DAC is clocked at frequencies approaching its upper operating limit, or as the DDS output frequency approaches one-half its clock rate, spurs caused by nonlinearities and glitch noise in the DAC become dominant. [Glitch noise is a ringing in the output waveform of the DAC as it transitions from one amplitude level to another. This noise worsens as (1) more current switches in the DAC change state simultaneously and (2) the time that the DAC is ringing becomes a large fraction of the total time that it stays at any particular state.] The technology for building DDSs at lower frequencies is more mature and allows for better spurious performance. At clock rates less than 100 MHz, a DDS can be built in low-power CMOS and can have a DAC with 10 bits, while 12-bit DACs are available at less than 50 MHz. At clock frequencies of 200 MHz to over 1 GHz, the devices are built in higher power emitter coupled logic (ECL) or GaAs, and the largest DACs available have only 8 bits. (Many manufacturers and foundries are chasing the elusive 1-GHz, 12-bit DAC.) Therefore, using a DDS for a synthesizer in an EHF system requires a full understanding of the spurious performance that can be expected from the DAC and the system requirements.

4.4 BANDWIDTH EXPANSION FOR A DIRECT DIGITAL SYNTHESIZER

A basic limitation of any DDS is the available bandwidth. As was discussed above, the output tuning range of a DDS is less than one-half the clock rate of the digital circuitry. To increase the frequency coverage to the range required for the EHF waveform, some method of bandwidth expansion must be employed. Two of the basic techniques for expanding the tuning range available at the synthesizer output are frequency multiplication and "offset mixing."

4.4.1 Frequency Multiplication

Frequency multiplication is the simplest method for obtaining bandwidth expansion. Putting the output of any portion of a synthesizer with bandwidth B into a times n multiplier yields a bandwidth of $(B * n)$ at the output of the multiplier, along with an associated reduction in resolution of $1/n$. The primary disadvantages of multipliers are that the noise and spurious from a DDS (after conversion to phase noise via the nonlinearity of a multiplier, amplifier, etc.) get enhanced by a factor of 20 log (n) dB as a side effect of the multiplication [5]. This enhancement can put a severe limitation on system performance. When using a DDS, it is prudent to limit the amount of frequency multiplication to a minimum in order to maintain a clean output signal.

4.4.2 Offset Mixing

Bandwidth expansion by "offset mixing" is simply the first half of a typical "mix-and-divide" stage from a direct analog synthesizer and is schematically represented in Figure 4. A DDS, which has a tuning

range of Δf, is mixed with a pure tone. This tone is a single frequency selected from a set of signals that are spaced at Δf. (These signals are typically harmonics produced by a comb generator.) By mixing the DDS with adjacent harmonics, an output bandwidth is produced that is an integer number of times broader than the DDS alone. The example in Figure 4 shows four harmonics that are mixed with a DDS to yield an output tuning range that is four times as wide as the DDS alone. This yields the same expansion as a times-4 multiplier but with no loss in resolution and without noise enhancement.

A simple and effective method of selecting a desired harmonic for offset mixing is to use a switchable filter bank (see Figure 5). A set of n band-pass filters is designed so that only one of the harmonics of the comb generator can pass through any one particular filter. Two n-way switches are used to route the set of harmonics from the comb generator through the appropriate filter, which results in a single frequency that is then applied to the offset mixer.

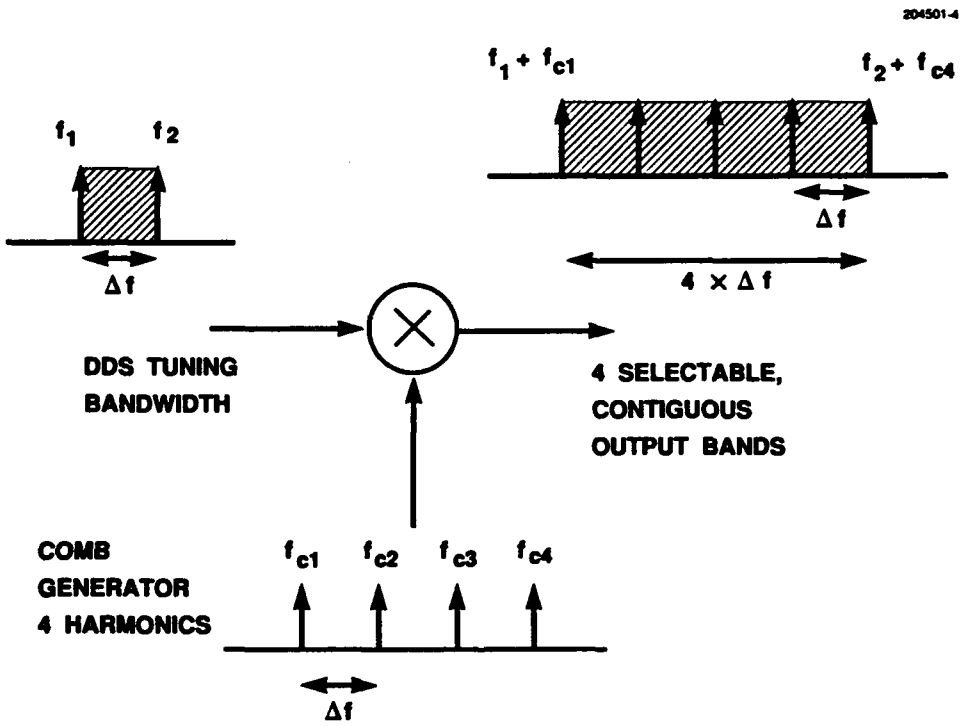


Figure 4. Bandwidth expansion by offset mixing.

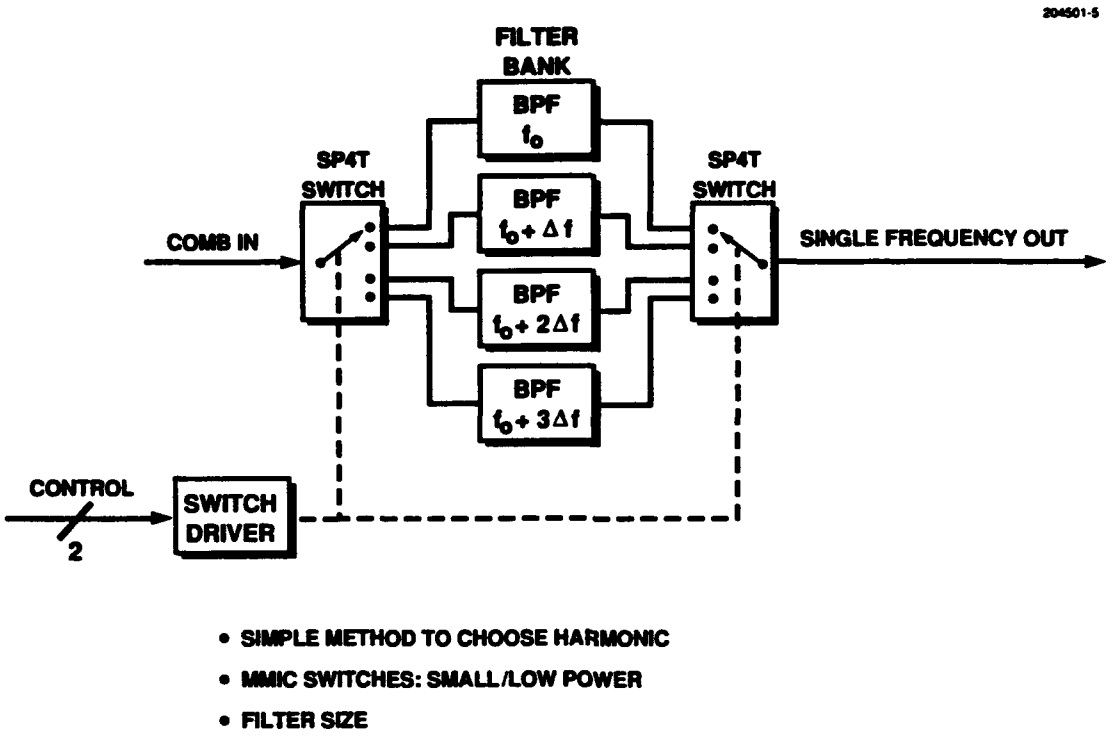


Figure 5. Switched filter bank block diagram.

GaAs FET switches built on MMIC circuits are readily available and can be used as the switching elements instead of the more common pin diodes. The FETs can switch as fast as pin diodes and because only gate voltage is applied to the FET (instead of forward current in the diodes), the drive circuitry requires virtually no bias current and is therefore an extremely low-power device.

Two disadvantages of using offset mixing are the size of the filter bank and the added complexity to the frequency plan. A trade-off must be made between the clock frequency, the tuning range of the DDS, its power consumption, and spurious versus the size and number of filters needed in the switched filter bank to accomplish the required bandwidth expansion. Also, the extra mixer requires that careful attention be paid to the frequency plan to ensure that no additional spurs are introduced into the signal path from Manley-Rowe products in the mixer itself.

5. DESIGN DETAILS

The RFG developed for ASCAMP is a hybrid of direct digital and direct analog design techniques. It consists of a DDS that provides 50 MHz of tuning range along with a frequency doubler and a six-channel switched filter bank (SFB) to accomplish the necessary bandwidth expansion.

A general block-diagram of the RFG is shown in Figure 6 and is typical of any synthesizer that is designed around a DDS. The fundamentals of the circuitry for the DDS and bandwidth expansion have already been described. Upconversion is required to achieve the desired synthesizer output frequency range. The reference circuitry sets the phase noise for the synthesizer. The LO distribution network generates the clock frequency for the DDS, the harmonics for the bandwidth expansion, and the LO signals for the upconverters. The degrees of freedom in designing the synthesizer were bound by the self-imposed requirement to make the RFG's output compatible with the SCOTT and original SCAMP frequency plans as well as the desire to use the highest frequency DDS available in order to minimize the bandwidth expansion required.

The RFG frequency plan was designed simultaneously with the frequency plans of the receiver and transmitter. This approach gave increased flexibility and allowed the design to incorporate significant simplifications relative to other MILSTAR terminals. The frequency command generation was implemented in digital hardware to easily accommodate any scaling and offsets in the frequency command word. Therefore, the constraint of an IF at 1.55 GHz, which had been a central design driver for previous terminal designs, could be ignored. Many other terminals maintain an IF in the receiver of 1.55 GHz to minimize the required tuning range of their synthesizer. Reducing tuning range is a critical consideration for a PLL-based synthesizer, but it was not as important to our design. Without this constraint, the design was based on the goal of minimizing the number of components and the design complexity. The cost of a slightly excessive tuning range was outweighed by the reduced number of components used to generate the fixed LO frequencies.

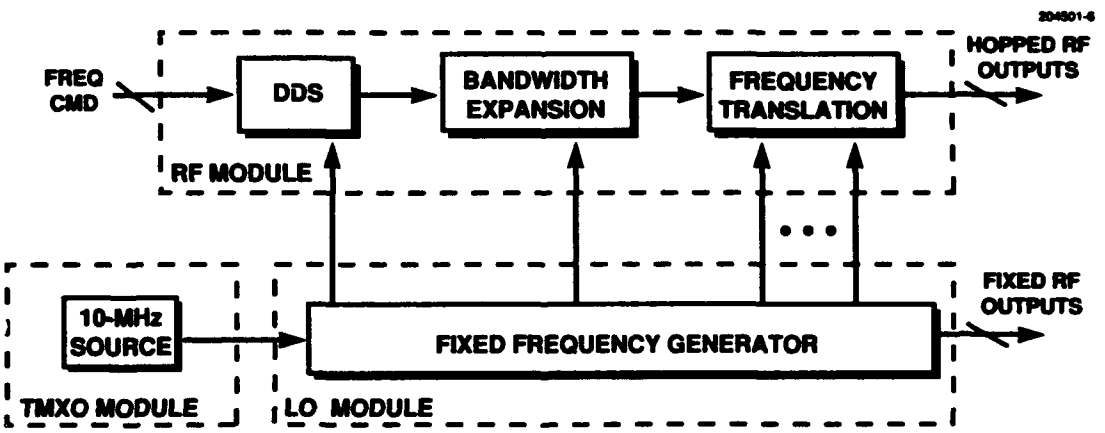


Figure 6. RF Generator conceptual block diagram.

5.1 FREQUENCY PLAN

The frequency plan of the RFG is shown in Figure 7. The design is based on a DDS that is clocked at 300 MHz and is tuned over a frequency range of 50 to 100 MHz. The DDS is followed by a frequency doubler to obtain a 100-MHz bandwidth. A six-channel SFB in combination with a 100-MHz comb generator provides the required bandwidth expansion to 600 MHZ of tuning range. The remaining mixers were chosen to minimize spur generation while converting the output to the proper frequency band.

The RFG and receiver IF were designed based on multiples of 100 MHz. The goal was to "reuse" frequencies wherever possible and to minimize the number of fixed frequencies required. The RFG provides an agile signal to the receiver and transmitter over a 10.8- to 11.4-GHz band. Note that the receiver and transmitter each use only a portion of the total available bandwidth, as shown in Figure 8. The RFG also provides fixed frequencies to the receiver of 1600 and 100 MHz, which are used as LO signals for the downconverter stages, and an 80-MHz signal to the digital system, which then is divided down and used for various clocks. Frequency plans for the receiver and transmitter are shown in Figures 9 and 10, respectively.

Close examination of the detailed frequency plan of the RFG, shown in Figure 7, further highlights the degree of simplicity and frequency reuse that this design employs. The reference for the entire RFG is based on a 10-MHz, vacuum-sealed, ovenized, crystal oscillator called the Tactical Miniature Crystal Oscillator (TMXO). The TMXO was developed at Bendix for the Army and is the same oscillator used in the original SCAMP and SCOTT terminals. (Because the TMXO is no longer being manufactured, future designs will have to incorporate alternate oscillators like the Efratom EMXO.) The 10-MHz source is frequency multiplied and the tenth harmonic (100 MHz) is then used as an intermediate frequency reference. (Note that the same multiplier is used to generate the 80-MHz tone used as a system clock by the digital subsystems.) A crystal filter is used to limit the noise bandwidth of the 100-MHz signal. This filter partially sets the phase noise of the RFG. The design simplicity of a crystal filter was utilized as opposed to relying on conventional techniques of PLLs. A PLL could have set the phase noise, and perhaps reduced the overall system noise to a small degree, but would have required more complex, more power-hungry circuitry, thereby reducing reproducibility and reliability while increasing cost.

5.2 FREQUENCY COMMANDS AND THE DIGITAL INTERFACE

This section will describe the method of commanding the RFG to a particular output frequency via its digital interface [6]. Algorithms for determining the frequency command, given a desired downlink or uplink frequency, are provided. As described in Section 5.1, the receiver and transmitter each use only a portion of the available output tuning range from the RFG. There are no specific controls or switches that change the state of the RFG between the transmit and receive modes. Commanding the RFG to output frequencies for the transmitter or receiver requires sending the appropriate frequency command to the RFG. When the receiver needs a specific frequency from the RFG, the transmitter gets that same signal (and vice versa). It is up to the ASCAMP controller circuitry to decide when the output of the receiver is valid and when the transmitter should be turned on or off.

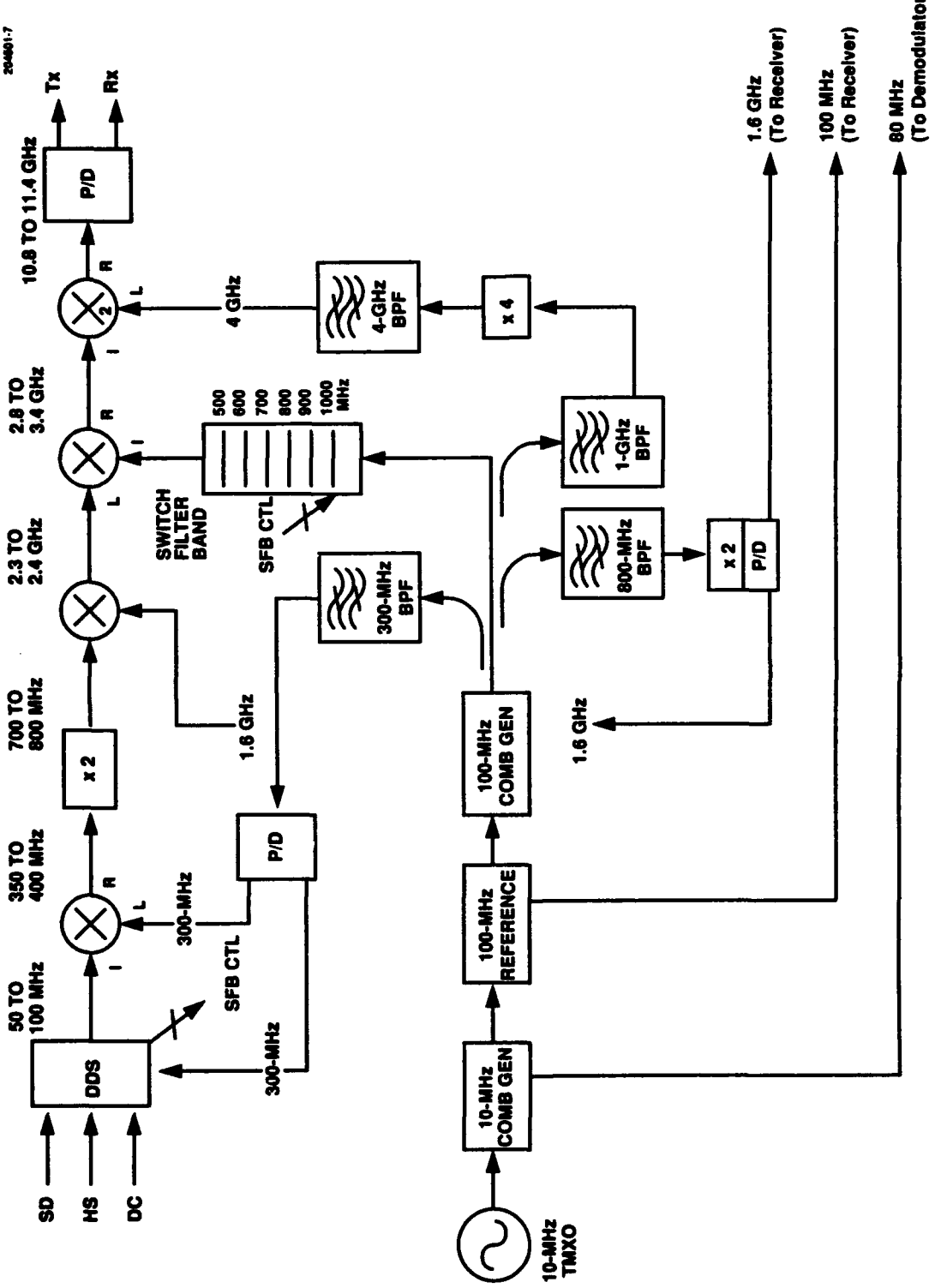


Figure 7. RF Generator frequency plan.

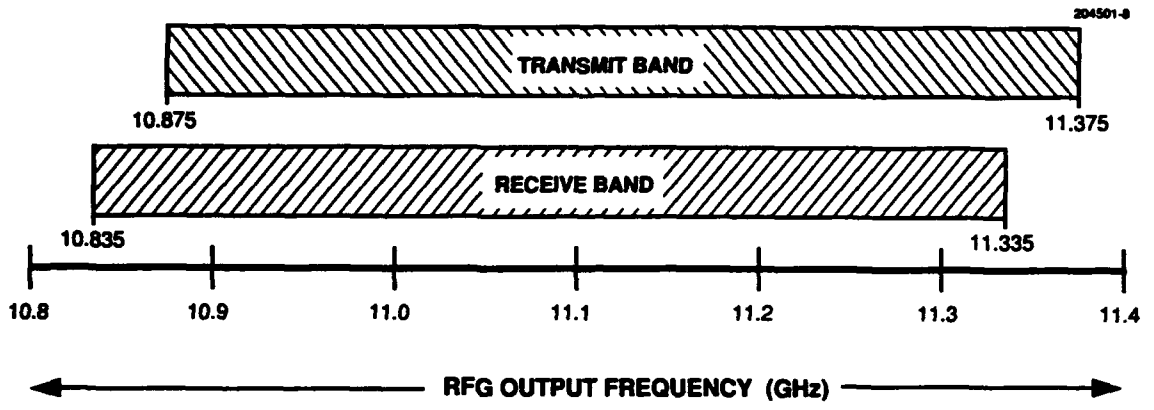


Figure 8. RF Generator output bandwidth.

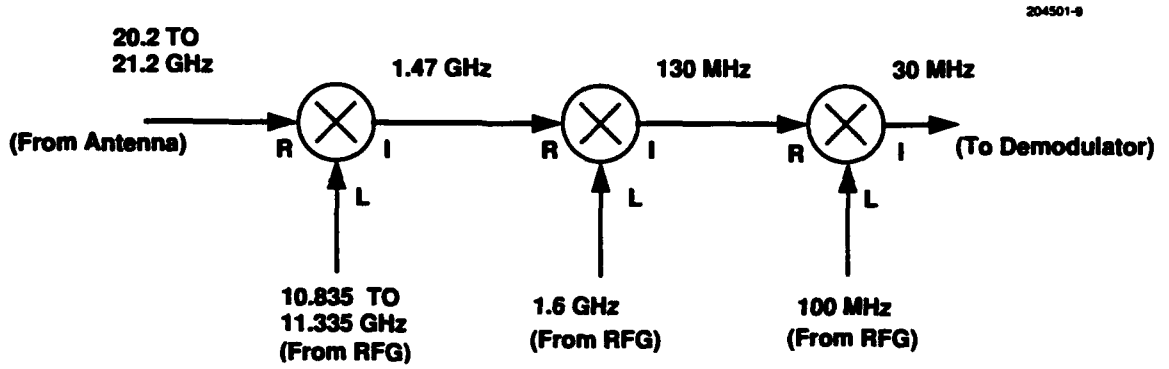


Figure 9. ASCAMP Receiver frequency plan.

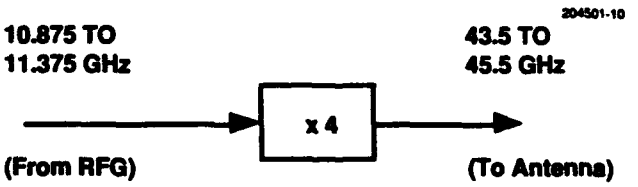


Figure 10. ASCAMP Transmitter frequency plan.

The output frequency of the RFG is set by the combination of the DDS frequency and the state of the SFB. The relationship of the RFG output frequency and the DDS frequency is given by the following equations.

$$f_{RFG} = \left(2 * f_{DDS}\right) + 10.2\ \text{GHz} + f_{SFB} \quad . \tag{3}$$

$$f_{DDS} = \frac{f_{RFG} - 10.2\ \text{GHz} + f_{SFB}}{2} \quad , \tag{4}$$

where

f_{DDS} = [50 through 100 MHz] (fine tuning)

f_{SFB} = [500, 600, 700, 800, 900, 1000 MHz] (frequency binning).

This relationship indicates the frequency binning that is required to tune the output of the RFG to a desired frequency. The DDS provides for fine tuning (with an effective frequency resolution of ≈ 2.2 Hz at the RFG's 11-GHz output), while the SFB provides coarse tuning in 100-MHz steps. A graphical summary of the frequency binning of the RFG's output bandwidth is shown in Figure 11. Note that not only is the algorithm for frequency conversion different during receive and transmit but that the frequency bins are not equally sized at the band edges.

The output frequency of the DDS is a function of the 28-bit frequency command (or increment) and the DDS clock frequency, as shown in Equation (5). Three bits control the state of the SFB and this relationship is shown in Tables 1 and 2.

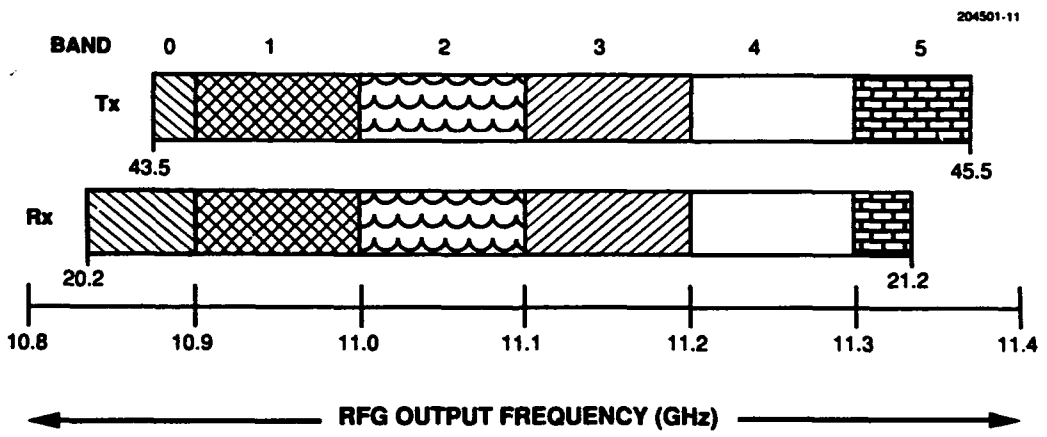


Figure 11. RF Generator frequency binning.

TABLE 1

RF Generator Frequency Binning for the Transmitter

f_{uplink} (GHz)	SFB Channel	SFB Control Bits	f_{SFB} (MHz)	f_{DDS} (MHz)
43.5 – 43.6	0	000	500	$f_{DDS} = \frac{f_{uplink}}{8} - 5.35\ GHz$
43.6 – 44.0	1	001	600	$f_{DDS} = \frac{f_{uplink}}{8} - 5.40\ GHz$
44.0 – 44.4	2	010	700	$f_{DDS} = \frac{f_{uplink}}{8} - 5.45\ GHz$
44.4 – 44.8	3	011	800	$f_{DDS} = \frac{f_{uplink}}{8} - 5.50\ GHz$
44.8 – 45.2	4	100	900	$f_{DDS} = \frac{f_{uplink}}{8} - 5.55\ GHz$
45.2 – 45.5	5	101	1000	$f_{DDS} = \frac{f_{uplink}}{8} - 5.60\ GHz$

$$f_{DDS} = \text{frq\_cmd} * \frac{f_{clock_{DDS}}}{2^N}$$

$$= \text{frq\_cmd} * \frac{300\ MHz}{2^{28}} \quad . \tag{5}$$

Three digital control signals are used to command the RFG to a desired frequency (see Figure 12). Serial data is a 31-bit serial data stream that contains 28 bits for the DDS frequency increment command and 3 bits to control the SFB. Data clock is a gated pulse train of 31, 1-μs pulses used to clock the serial data into the RFG. Hop sync is a 900-ns wide pulse that synchronizes the data transfer with the beginning of every hop.

As shown in Figure 12, there is an unspecified time delay (100 ns ≤ t_d ≤ 10 μs) between hop sync's rising edge and the beginning of the gated clock and data stream. This delay allows for the data to be synchronously transferred from the controlling device to the RFG's DDS board without concern for small time variations or device delays in the controller. This transfer of the frequency command data *must* take place during the hop *before* the new frequency is required at the RFG output. In other words, transferring the frequency command by a serial data line requires a *one hop set up time* for the data to be transferred serially, converted to parallel, and latched to the parallel input ports of the DDS. This serial-to-parallel conversion in done in the Xilinx chip on the DDS board in the RFG.

TABLE 2

RF Generator Frequency Binning for the Receiver

$f_{downlink}$ (GHz)	SFB Channel	SFB Control Bits	f_{SFB} (MHz)	f_{DDS} (MHz)
20.2 – 20.33	0	000	500	$f_{DDS} = \frac{f_{downlink}}{4} - 4.9825$ GHz
20.33 – 20.53	1	001	600	$f_{DDS} = \frac{f_{downlink}}{4} - 5.0325$ GHz
20.53 – 20.73	2	010	700	$f_{DDS} = \frac{f_{downlink}}{4} - 5.0825$ GHz
20.73 – 20.93	3	011	800	$f_{DDS} = \frac{f_{downlink}}{4} - 5.1325$ GHz
20.93 – 21.13	4	100	900	$f_{DDS} = \frac{f_{downlink}}{4} - 5.1825$ GHz
21.13 – 21.20	5	101	1000	$f_{DDS} = \frac{f_{downlink}}{4} - 5.2325$ GHz

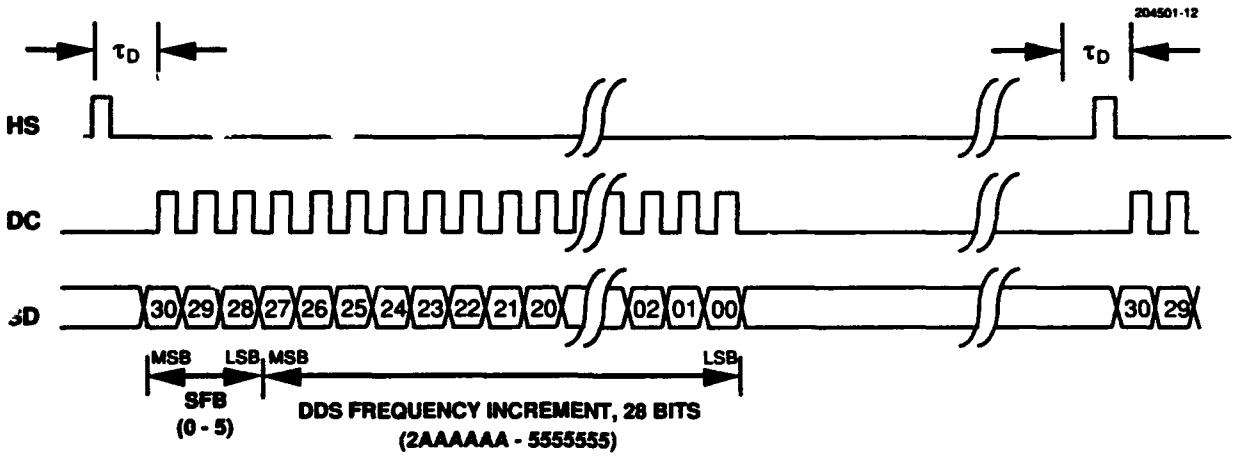


Figure 12. RF Generator frequency command interface.

5.2.1 RFG Frequencies and the Transmitter

A frequency plan of the ASCAMP transmitter was shown above in Figure 10. The 11-GHz hopping output from the RFG is frequency multiplied by four, then amplified and sent directly to the uplink feedhorn of the antenna. Equation (6) is used to calculate the required RFG frequency given a desired uplink frequency. The result of combining Equations (4) and (6) is shown in Table 1, which provides the frequency binning to determine the required DDS and SFB frequencies for a desired uplink frequency.

$$f_{RFG} = \frac{f_{uplink}}{4} \quad . \tag{6}$$

5.2.2 RFG Frequencies and the Receiver

A frequency plan of the ASCAMP receiver was shown in Figure 9. The 11-GHz signal from the RFG provides a hopping, high-side LO to the receiver's first downconversion, such that the output from the first mixer is a fixed frequency at 1.47 GHz (plus any modulation). Equation (7) is used to calculate the required RFG frequency given a downlink frequency. The result of combining Equations (4) and (7) is shown in Table 2, which provides the frequency binning to determine the required DDS and SFB frequencies for a desired downlink frequency.

$$f_{RFG} = \frac{f_{downlink} + 1.47\,\text{GHz}}{2} \quad . \tag{7}$$

5.3 MIXER SPURIOUS ANALYSES

This section will describe the spurious analyses that were performed on the hopping signal path from the first upconversion after the DDS to the final 11-GHz output of the RFG. The design of this rf signal path had to include the required bandwidth expansion and frequency shifting of the tuning range to the required output frequency band.

The starting point of the design was the 10.8- to 11.4-GHz output band as well as the available tuning range from the DDS. The DDS was determined to have approximately 72 MHz of available range, based on tuning the DDS between 10% and 40% of its clock frequency. (Note that the original design was made to accommodate a DDS clock frequency of only 240 MHz.) The first mixer was needed to upconvert the tuning band of the DDS away from dc. This allowed for a reasonable design for the band-pass filter in the first IF section. The last mixer was intended to minimize the amount of circuitry needed to function at X-band. The middle two upconversion stages were the result of trade-offs in filter and spurious requirements and the desire to reuse whatever frequencies *had* to be generated in the RFG.

The final frequency plan was reached after numerous trade-off studies between expected spurious from the mixers, filter requirements, and circuitry designs that would be required to generate fixed LO signals. During this phase, the filters were designed simultaneously with the frequency plan itself.

Following a description of each upconversion stage is a chart showing an analysis of the Manley-Rowe spurious for that mixer. The column labeled "IB/OB" indicates which spurs would fall in-band or out-of-band (any spurs at the band edge are considered in-band). The column labeled "Est Level" is a very rough approximation of the spurious level, in dBc, from a typical mixer driven with an IF at −10 dBm and an LO drive of +7 dBm. These spurious levels were extracted from manufacturers' data sheets. The last column marks the spurs that were considered potentially problematic and therefore determines filter requirements or those spurs that would limit system performance.

Accompanying each chart of Manley-Rowe spurs is a plot that shows the measured values of the spurious for each mixer, as measured in a test fixture. It was expected that spurious levels would vary somewhat after being installed in the actual circuits due to actual signal levels and mismatching with cascaded components. Where spurious signals were expected with relatively high levels, extra care was taken during the assembly and tuning to set rf signal levels to minimize the spurs.

5.3.1 Mixer 1

The DDS output of 50 to 100 MHz is fed into the X-port of an MD-169 mixer with an LO at 300 MHz. The LO signal is obtained from one side of a power divider in the LO Board of the LO Module. (Note that the other side of the power divider is used as the clock signal in the DDS board. This is the first instance of frequency reuse in the RFG.) The goal for this mixer is to get the rf tuning bandwidth as far from dc as possible without making the band-pass filter that follows the mixer too hard to fabricate. By shifting the tuning range away from dc, the relative bandwidth is reduced from an octave to less than 15%. This reduction allows for a reasonable filter design. Although using an even higher frequency LO would further reduce the percentage bandwidth, the LO rejection would be harder to achieve in the first IF band-pass filter. Table 3 is a chart of the Manley-Rowe spurious analysis. Figure 13 is a plot of the spurious for this mixer measured in a test fixture.

5.3.2 Mixer 2

After the rf signal is frequency doubled, mixer 2 shifts the tuning band to S-band. This shift further reduces the percentage bandwidth while keeping the operating frequency below 4 GHz where amplifier gain is easy to implement. The mixing signal for this converter is generated by the same circuitry that generates the 1.6-GHz LO for the receiver, which is another instance of frequency reuse. Unfortunately, this mixer would suffer from an intolerable in-band spur if it was implemented as a normal upconverter with 1.6 GHz as the LO signal. A standard Manley-Rowe analysis would predict a (−1,2) that falls in-band, which would limit system performance. To eliminate this problem, we incorporated a technique [7] to reduce the level of undesired mixer spurs. Instead of pumping the high-level 1.6-GHz signal into the LO port of the mixer and the low-level UHF signal into the IF port, the mixer ports were reversed (i.e., the high-level 1.6-GHz signal was injected to the IF port and the low-level UHF signal was injected into the LO port). This method is effective in reducing the level of the (−1,2) spur at the mixer's output port due to the internal balanced topology of the mixer's LO port [8]. The side effect of implementing this technique is that the (2,1) spur is not suppressed. However, because the (2,1) spur is far out-of-band, it can easily be filtered. Empirical evidence of this method is demonstrated in Figures 14(a) and (b). Figure 14(a) shows the measured spurious with the

mixer used in the usual way and the (–1,2) spur is approximately –35 dBc. Figure 14(b) shows data taken with the mixer ports reversed and the (–1,2) spur is below the noise floor of –55 dBc. Table 4 is a chart of the Manley-Rowe spurious analysis with expected spur levels based on the "reversed-port" topology.

TABLE 3

Mixer 1 Manley-Rowe Spurious Analyses

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
–5 2	50	300	350	IB	>70
–5 2	100	300	100		
–5 3	50	300	650	IB	>70
–5 3	100	300	400		
–4 2	50	300	400	IB	>70
–4 2	100	300	200		
–4 3	50	300	700	OB	>70
–4 3	100	300	500		
–3 2	50	300	450	IB	>60
–3 2	100	300	300		
–2 2	50	300	500	IB	>70
–2 2	100	300	400		
–1 2	50	300	550	OB	~37*
–1 2	100	300	500		
1 1	50	300	350	Desired	0
1 1	100	300	400		
2 1	50	300	400	IB	>60
2 1	100	300	500		
3 1	50	300	450	OB	>50
3 1	100	300	600		
4 0	50	300	200	IB	>60
4 0	100	300	400		
4 1	50	300	500	OB	>60
4 1	100	300	700		
5 0	50	300	250	IB	>60
5 0	100	300	500		

* Determines filter requirements or mixer performance
Spurs in defined BW = 310 to 490 MHz. Max mode: 5

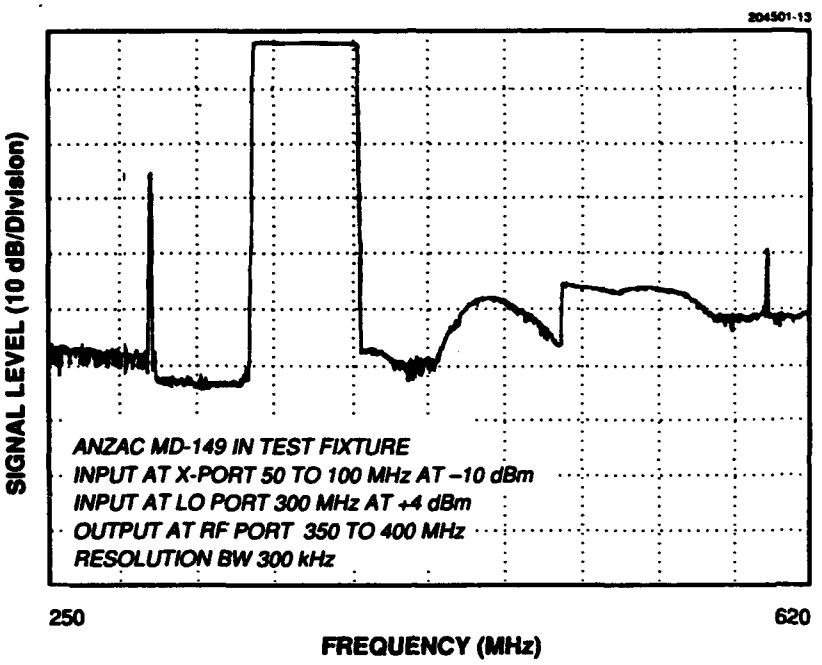


Figure 13. Measured spurious for mixer 1.

5.3.3 Mixer 3

This mixer is used to accomplish a sixfold bandwidth expansion. The mixer takes a tuning bandwidth of 100 MHz and, via the technique of offset mixing described previously, produces an output tuning range of 600 MHz. A fixed frequency of 500, 600, 700, 800, 900, or 1000 MHz is mixed with the rf signal path tuning range of 2.3 to 2.4 GHz to yield an output tuning range of 2.8 to 3.4 GHz. The Manley-Rowe charts (see Tables 5 to 10) provide a separate analysis for every fixed frequency used in the mixer. This mixer suffers from in-band spurs similar to mixer 2; the worst spur is the (0,3) spur with a fixed mixing frequency of 1000 MHz. To eliminate this problem, the 2.3- to 2.4-GHz signal is amplified and used to pump the LO port of the mixer while the fixed frequencies are injected at low levels into the IF port. The level of the in-band spurs is reduced to acceptable levels, as shown in Figures 15(a) to (f). The worst in-band spur is now a (–2,2) spur whose level can be reduced to less than –45 dBc by adjusting the IF drive level. (Note that the Manley-Rowe charts list the estimated spur levels based on the 2.3- to 2.4-GHz signal being used as an LO.)

5.3.4 Mixer 4

This mixer is the final upconversion stage in the RFG and shifts the full 600-MHz tuning range to the desired 10.8- to 11.4-GHz bandwidth. The converter is a harmonic mixer that takes a 4-GHz LO and, due to its internal circuit topology, produces a dominant (1,2) product, thereby acting as if it had an 8-GHz LO. The Manley-Rowe chart in Table 11 shows that the (–3,5) is the dominant in-band spur. The measured data of the mixer in Figure 16 shows the spur level to be better than –40 dBc.

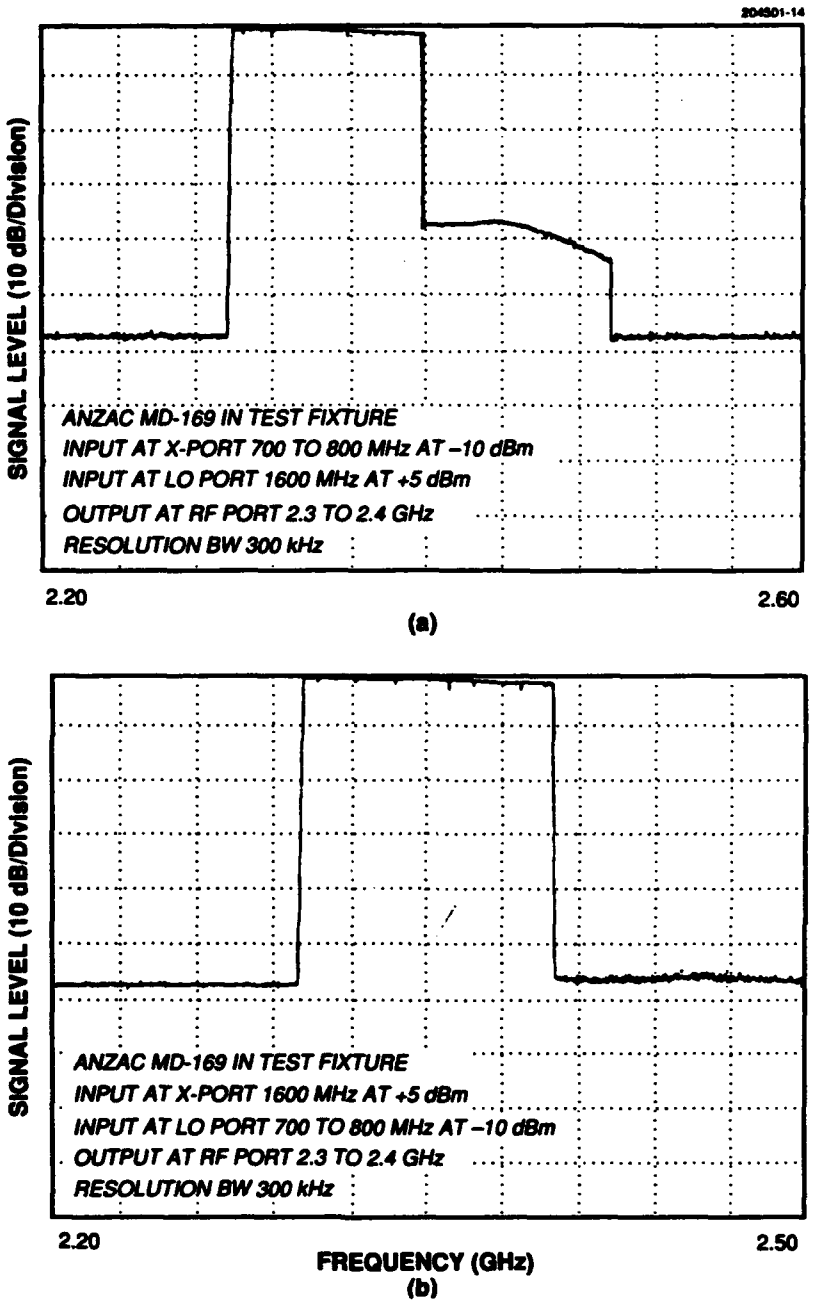


Figure 14. Measured spurious for mixer 2 (a) standard topology and (b) reversed port topology.

TABLE 4

Mixer 2 Manley-Rowe Spurious Analyses

(M × N)	Fin*	FLO*	Fspur	IB/OB	Est Level
–5 4	0.7	1.6	2.9	IB	>70
–5 4	0.8	1.6	2.4		
–4 3	0.7	1.6	2.0	OB	>70
–4 3	0.8	1.6	1.6		
–3 3	0.7	1.6	2.7	IB	>50*
–3 3	0.8	1.6	2.4		
–2 2	0.7	1.6	1.8	OB	>60
–2 2	0.8	1.6	1.6		
–1 2	0.7	1.6	2.5	IB	>60
–1 2	0.8	1.6	2.4		
1 1	0.7	1.6	2.3	Desired	0
1 1	0.8	1.6	2.4		
2 1	0.7	1.6	3.0	OB	~35
2 1	0.8	1.6	3.2		
3 0	0.7	1.6	2.1	IB	>60
3 0	0.8	1.6	2.4		
4 0	0.7	1.6	2.8	OB	>60
4 0	0.8	1.6	3.2		
5 –1	0.7	1.6	1.9	IB	>70
5 –1	0.8	1.6	2.4		

* Determines filter requirements or mixer performance
Spurs in defined BW = 1.7 to 3.1 GHz. Max mode: 5
Reversed topology

TABLE 5

Mixer 3 Manley-Rowe Spurious Analyses (500-MHz Fixed Frequency)

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
5 0	500	2300	2500	OB	>70
5 0	500	2400	2500		
0 1	500	2300	2300	OB	~25*
0 1	500	2400	2400		
1 1	500	2300	2800	Desired	0
1 1	500	2400	2900		
2 1	500	2300	3300	IB	>70
2 1	500	2400	3400		
3 1	500	2300	3800	OB	>60
3 1	500	2400	3900		
4 1	500	2300	4300	OB	>70
4 1	500	2400	4400		
–5 2	500	2300	2100	OB	>70
–5 2	500	2400	2300		
–4 2	500	2300	2600	IB	>70
–4 2	500	2400	2800		
–3 2	500	2300	3100	IB	>60
–3 2	500	2400	3300		
–2 2	500	2300	3600	OB	>70
–2 2	500	2400	3800		
–1 2	500	2300	4100	OB	~35
–1 2	500	2400	4300		
–5 3	500	2300	4400	OB	>70
–5 3	500	2400	4700		

* Determines filter requirements or mixer performance
Spurs in defined BW = 2 to 4.5 MHz. Max mode: 5

TABLE 6

Mixer 3 Manley-Rowe Spurious Analyses (600-MHz Fixed Frequency)

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
4 0	600	2300	2400	OB	>70
4 0	600	2400	2400		
5 0	600	2300	3000	IB	>70
5 0	600	2400	3000		
0 1	600	2300	2300	OB	~25*
0 1	600	2400	2400		
1 1	600	2300	2900	Desired	0
1 1	600	2400	3000		
2 1	600	2300	3500	OB	>70
2 1	600	2400	3600		
3 1	600	2300	4100	OB	>60
3 1	600	2400	4200		
–4 2	600	2300	2200	OB	>60
–4 2	600	2400	2400		
–3 2	600	2300	2800	IB	>60
–3 2	600	2400	3000		
–2 2	600	2300	3400	IB	>70
–2 2	600	2400	3600		
–1 2	600	2300	4000	OB	~35*
–1 2	600	2400	4200		
–5 3	600	2300	3900	OB	>70
–5 3	600	2400	4200		
–4 3	600	2300	4500	OB	>70
–4 3	600	2400	4800		

* Determines filter requirements or mixer performance
Spurs in defined BW = 2 to 4.5 MHz. Max mode: 5

TABLE 7

Mixer 3 Manley-Rowe Spurious Analyses (700-MHz Fixed Frequency)

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
3 0	700	2300	2100	OB	>60
3 0	700	2400	2100		
4 0	700	2300	2800	IB	>70
4 0	700	2400	2800		
5 0	700	2300	3500	OB	>70
5 0	700	2400	3500		
0 1	700	2300	2300	OB	~25*
0 1	700	2400	2400		
1 1	700	2300	3000	Desired	0
1 1	700	2400	3100		
2 1	700	2300	3700	IB	>70
2 1	700	2400	3800		
3 1	700	2300	4400	OB	>60
3 1	700	2400	4500		
–3 2	700	2300	2500	OB	>60
–3 2	700	2400	2700		
–2 2	700	2300	3200	IB	>70
–2 2	700	2400	3400		
–1 2	700	2300	3900	OB	~35*
–1 2	700	2400	4100		
–5 3	700	2300	3400	IB	>70
–5 3	700	2400	3700		
–4 3	700	2300	4100	OB	>70
–4 3	700	2400	4400		

* Determines filter requirements or mixer performance
Spurs in defined BW = 2 to 4.5 MHz. Max mode: 5

TABLE 8

Mixer 3 Manley-Rowe Spurious Analyses (800-MHz Fixed Frequency)

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
3 0	800	2300	2400	OB	>60
3 0	800	2400	2400		
4 0	800	2300	3200	IB	>70
4 0	800	2400	3200		
5 0	800	2300	4000	OB	>70
5 0	800	2400	4000		
0 1	800	2300	2300	OB	~25*
0 1	800	2400	2400		
1 1	800	2300	3100	Desired	0
1 1	800	2400	3200		
2 1	800	2300	3900	OB	>70
2 1	800	2400	4000		
–3 2	800	2300	2200	OB	>60
–3 2	800	2400	2400		
–2 2	800	2300	3000	IB	>70
–2 2	800	2400	3200		
–1 2	800	2300	3800	OB	~35*
–1 2	800	2400	4000		
–5 3	800	2300	2900	IB	>70
–5 3	800	2400	3200		
–4 3	800	2300	3700	OB	>70
–4 3	800	2400	4000		
–3 3	800	2300	4500	OB	~50
–3 3	800	2400	4800		

* Determines filter requirements or mixer performance
Spurs in defined BW = 2 to 4.5 MHz. Max mode: 5

TABLE 9

Mixer 3 Manley-Rowe Spurious Analyses (900-MHz Fixed Frequency)

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
5 –1	900	2300	2200	OB	>70
5 –1	900	2400	2100		
3 0	900	2300	2700	OB	>60
3 0	900	2400	2700		
4 0	900	2300	3600	OB	>70
4 0	900	2400	3600		
5 0	900	2300	4500	OB	>70
5 0	900	2400	4500		
0 1	900	2300	2300	OB	~25*
0 1	900	2400	2400		
1 1	900	2300	3200	Desired	0
1 1	900	2400	3300		
2 1	900	2300	4100	OB	>70
2 1	900	2400	4200		
–3 2	900	2300	1900	OB	>60
–3 2	900	2400	2100		
–2 2	900	2300	2800	IB	>70
–2 2	900	2400	3000		
–1 2	900	2300	3700	OB	~35*
–1 2	900	2400	3900		
–5 3	900	2300	2400	OB	>70
–5 3	900	2400	2700		
–4 3	900	2300	3300	IB	>70
–4 3	900	2400	3600		
–3 3	900	2300	4200	OB	~50
–3 3	900	2400	4500		

* Determines filter requirements or mixer performance
Spurs in defined BW = 2 to 4.5 MHz. Max mode: 5

TABLE 10

Mixer 3 Manley-Rowe Spurious Analyses (1000-MHz Fixed Frequency)

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
5 –1	1000	2300	2700	OB	>70
5 –1	1000	2400	2600		
3 0	1000	2300	3000	IB	>60
3 0	1000	2400	3000		
4 0	1000	2300	4000	OB	>70
4 0	1000	2400	4000		
0 1	1000	2300	2300	OB	~25*
0 1	1000	2400	2400		
1 1	1000	2300	3300	Desired	0
1 1	1000	2400	3400		
2 1	1000	2300	4300	OB	>70
2 1	1000	2400	4400		
–2 2	1000	2300	2600	IB	>70
–2 2	1000	2400	2800		
–1 2	1000	2300	3600	OB	~35*
–1 2	1000	2400	3800		
–5 3	1000	2300	1900	OB	>70
–5 3	1000	2400	2200		
–4 3	1000	2300	2900	IB	>70
–4 3	1000	2400	3200		
–3 3	1000	2300	3900	OB	~50
–3 3	1000	2400	4200		
–5 4	1000	2300	4200	OB	>70
–5 4	1000	2400	4600		

* Determines filter requirements or mixer performance
Spurs in defined BW = 2 to 4.5 MHz. Max mode: 5

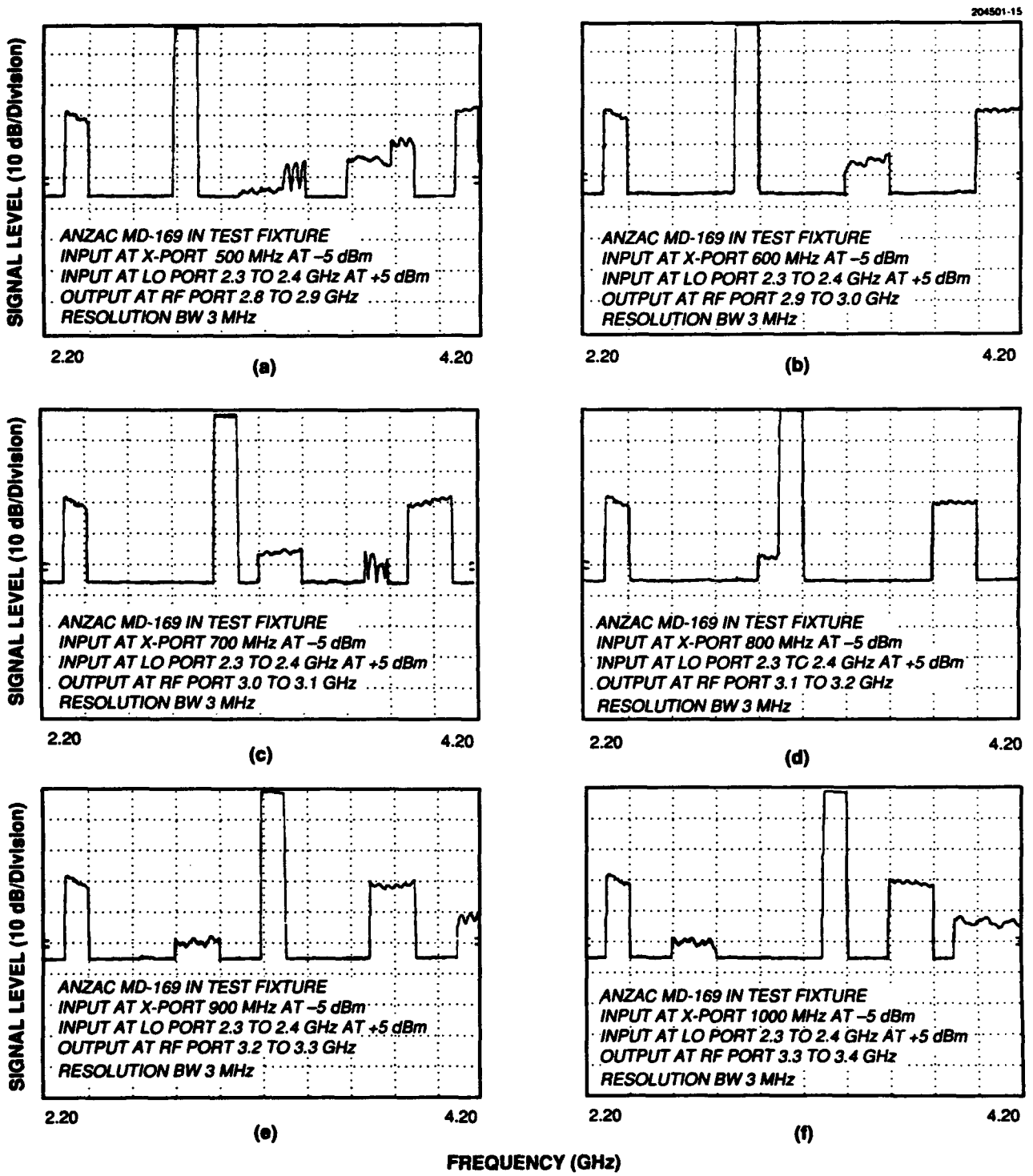


Figure 15. Measured spurious for mixer 3 (a) 500-MHz IF, (b) 600-MHz IF, (c) 700-MHz IF, (d) 800-MHz IF, (e) 900-MHz IF, and (f) 1000-MHz IF.

TABLE 11

Mixer 4 Manley-Rowe Spurious Analyses

(M × N)	Fin	FLO	Fspur	IB/OB	Est Level
−3 5	2.8	4	11.6	IB	~45*
−3 5	3.4	4	9.8		
−2 4	2.8	4	10.4	OB	>70
−2 4	3.4	4	9.2		
0 3	2.8	4	12.0	OB	~40*
0 3	3.4	4	12.0		
1 2	2.8	4	10.8	Desired	0
1 2	3.4	4	11.4		
2 1	2.8	4	9.6	IB	>70
2 1	3.4	4	10.8		
3 0	2.8	4	8.4	OB	>60
3 0	3.4	4	10.2		
4 0	2.8	4	11.2	IB	>70
4 0	3.4	4	13.6		
5 −1	2.8	4	10.0	IB	>70
5 −1	3.4	4	13.0		

* Determines filter requirements or mixer performance
Spurs in defined BW = 10 to 12.2 MHz. Max mode: 5

5.4 PHASE NOISE ANALYSIS

5.4.1 Original Design Concept and Analysis

The original SCAMP synthesizer used a high-order frequency multiplier chain to expand its tuning range to the desired output bandwidth. The phase noise of the system's 10-MHz source was enhanced by this same multiplier chain due to the design's architecture. This enhancement meant that noise reduction techniques that involved limiting the noise bandwidth could not be implemented due to the wide bandwidth of the RFG's tuning range.

The design architecture and frequency plan of the ASCAMP RFG separate the rf signal path from the phase noise path. Due to the low order of frequency multiplication from the DDS to the RFG's output, the phase noise in the rf signal path has a negligible contribution to the total system noise. (However,

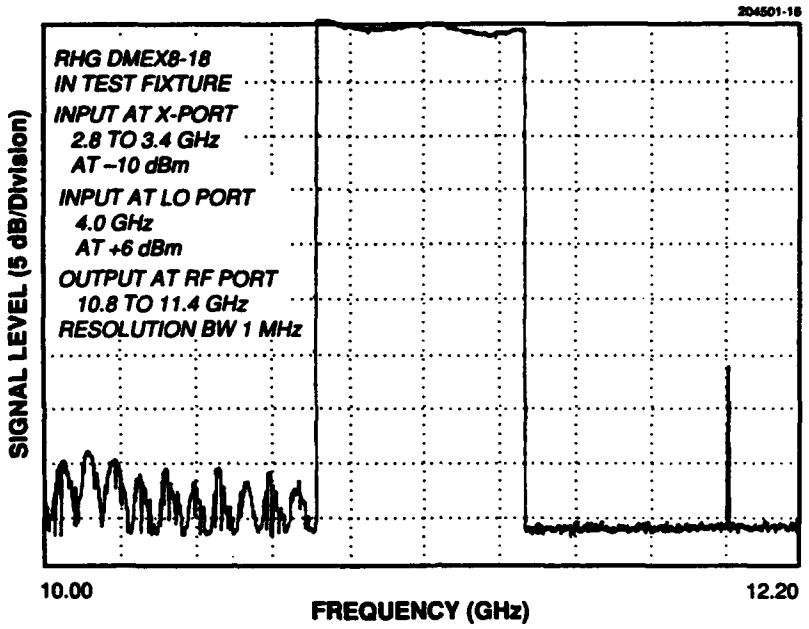


Figure 16. Measured spurious for mixer 4.

as noted elsewhere, the rf signal path is the major contributor of noise due to discrete spurious signals.) The signal path that sets the phase noise in the ASCAMP RFG originates in the TMXO, is processed in a multiplier chain in the fixed frequency generator, and then gets mixed in with the rf signal path at the final upconversion stage of the RFG. It should be noted that there is still the inescapable enhancement of phase noise from frequency multiplication due to the ratio of the 10-MHz system reference to the effective 8-GHz signal at the last mixer's LO port.

$$\text{Phase Noise Enhancement} = 20 * \log_{10}(\text{multiplication factor})$$

$$= 20 * \log_{10}\left(\frac{8\ \text{GHz}}{10\ \text{MHz}}\right) = 58\ \text{dB} \quad . \tag{8}$$

If the entire noise bandwidth from the TMXO was actually allowed to be enhanced by this factor, then the desired carrier signal would be suppressed by noise at the output of the RFG and transmitter. Therefore, it is still imperative to provide some means to reduce the total amount of phase noise.

During the preliminary design of the RFG, we were planning to use the classical approach for reducing phase noise in a multiplier chain. This approach involves using a PLL with a very narrow loop bandwidth at an intermediate frequency in the multiplier chain. Our initial design was going to incorporate either a surface acoustic wave (SAW) oscillator or a SAW resonator in a PLL. After evaluating the design alternatives, we chose to replace the PLL with a design incorporating a CMOS comb generator

and a crystal band-pass filter. A crystal filter with a noise bandwidth comparable to the loop bandwidth of a PLL could provide equivalent functionality with much less dc power and a much less complex, more reproducible circuit.

A frequency multiplier/comb generator was developed that was implemented in digital devices [9]. This circuit was used to generate a family of harmonics from the 10-MHz TMXO and to filter off the 100-MHz tone with the crystal filter. The result is that the phase noise was now set at an intermediate frequency in the multiplier chain. A preliminary phase noise analysis [10] verified the validity of this design approach. That analysis was based on the following set of ground rules and assumptions.

1. Analysis was performed for a terminal operating in low hop rate mode because this mode has the narrowest demodulator bandwidth and therefore the most stringent synthesizer phase noise requirement.
2. The *total noise power* at the transmitter output must be at least 20 dB below the signal level (to cause less than 0.05 dB of carrier suppression); this drives the system phase noise requirement.
3. Due to the demodulator bandwidth, any phase noise (or spurious) within ~500 Hz of the carrier is indistinguishable from the signal itself.
4. The 100-MHz crystal filter following the times-10 CMOS multiplier has a "brick wall" bandwidth of 10 kHz. (The actual filter used will be described below.)
5. The CMOS comb generator can be modeled as having a flat phase noise characteristic for all offset frequencies from the carrier greater than 500 Hz.
6. The total phase noise of the RFG is dominated by the phase noise set at the 100-MHz reference point (i.e., noise contributions from "downstream" circuitry would be negligible).

To verify that the multiplier/filter design would provide adequate phase noise, the following preliminary analysis was conducted. The phase noise from the 100-MHz reference point is enhanced along the signal path, as shown in Table 12 (also see the frequency plan in Figure 7).

Therefore, to maintain the CNR at the transmitter output (due to phase noise in the RFG) in excess of 20 dB, the total phase noise at the 100-MHz reference must be

$$\text{Total Phase Noise}_{\text{relative to carrier}} \geq -20 \text{ dBc} - 50.1 \text{ dB} \geq -70.1 \text{ dBc} \quad . \tag{9}$$

Given the above assumptions of the demodulator and crystal filter bandwidths, the phase noise at 100 MHz (measured in dBc/Hz) needs to be integrated over

$$9 \text{ kHz} = (10 \text{ kHz XBPF bandwidth} - 1 \text{ kHz demodulator bandwidth}) \quad , \tag{10}$$

where

$$\begin{aligned} \text{Bandwidth}_{\text{dB}} &= 10 * \log_{10} \left(\text{Bandwidth}_{\text{Hz}} \right) \\ &= 10 * \log_{10} (9e3) = 39.5 \text{ dB} \quad . \end{aligned} \tag{11}$$

TABLE 12

Phase Noise Enhancement Path

Input Frequency	Frequency Multiplication Factor	Output Frequency	Circuitry	Phase Noise Enhancement
100 MHz	× 10	1 GHz	Comb generator	20.00 dB
1 GHz	× 4	4 GHz	Quadrupler	12.04 dB
4 GHz	× 2	8 GHz (LO) (RFG output)	Harmonic mixer	6.02 dB
RFG Output	× 4	44 GHz	Transmitter front end	12.04
Total phase noise enhancement				50.10 dB

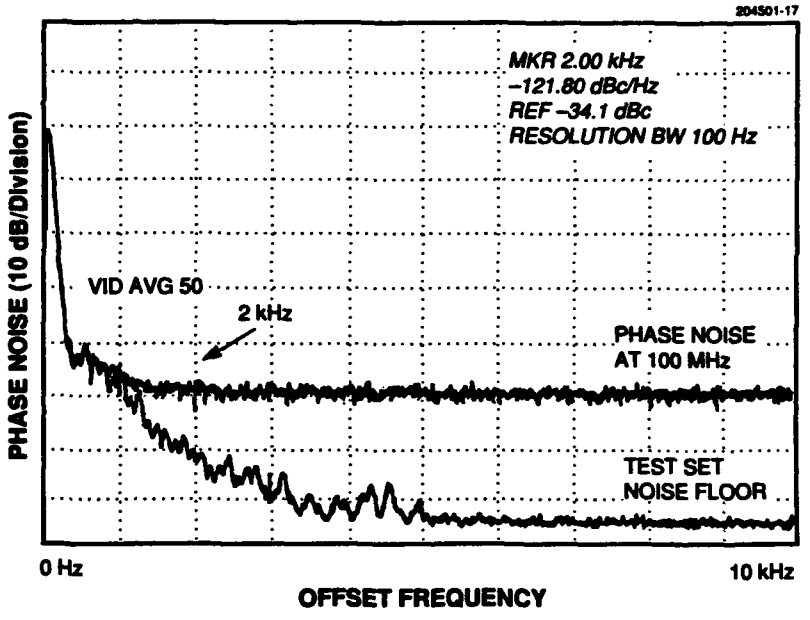


Figure 17. Phase noise of 10-MHz comb generator.

This results in the specification for the phase noise at 100 MHz to be equivalent to a flat noise floor at carrier offsets between 500 Hz and 10 kHz of

$$L_f = -70.1 \text{ dBc} - 39.5 \text{ dB} - 3 \text{ dB} = -112.6 \text{ dBc/Hz} \quad . \tag{12}$$

where the additional factor of 3 dB accounts for double-sided phase noise (i.e., integrating the noise over ±10 kHz from the carrier, excluding ±500 Hz).

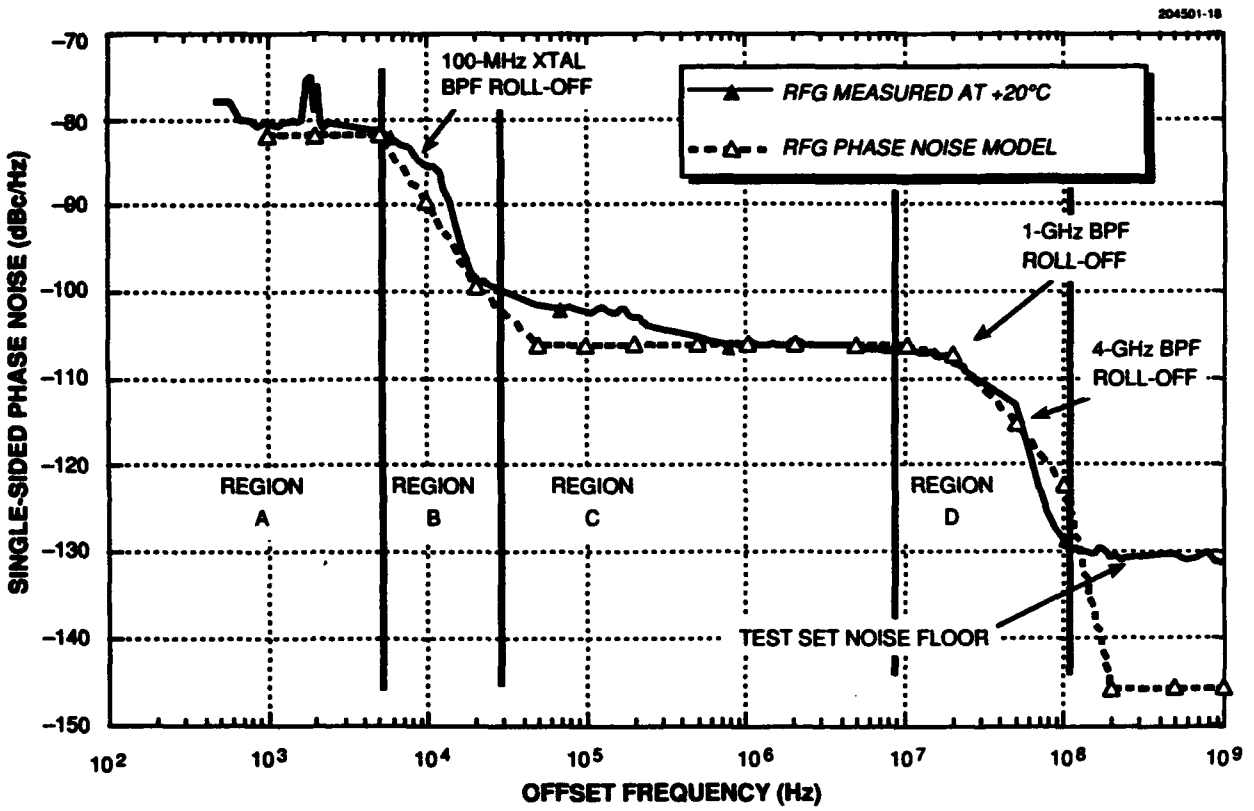
Measured [10] phase noise of a CMOS times-10 multiplier and a 100-MHz reference board (see Figure 17) verified the flat noise characteristic of the digital device and showed that a PLL source, with all of its inherent complexities, would not be necessary for the ASCAMP RFG. (Details of the phase noise test methodology are described in a following section.)

5.4.2 Analysis of a Complete RFG

A more thorough phase noise analysis was performed that takes into account all the components in the RFG: signal levels, components' gain and loss figures, and individual noise contributions. This analysis [11] was performed within the framework of a spreadsheet in order to perform numerous computations and integrations for the different components and to analyze the effect of changes in component parameters. A condensed printout of the analysis is shown in Table 13(a–d), and the measured frequency response of the critical filters used in the analysis is listed in Table 13(e). A plot that compares the measured versus predicted phase noise is shown in Figure 18. The model and analysis will be described next, while the test set for measuring the actual phase noise is detailed in a later section.

The model defines the signal path that sets the phase noise for the RFG. The model starts with the TMXO, which is the 10-MHz source oscillator for the RFG. Each downstream component in the signal path is represented with a column that defines the component's parameters that affect the signal level and the noise. The columns modeling the components are alternated with data columns that calculate the predicted signal and noise levels at each stage along the signal path. Table 14 describes the component parameter models, and Table 15 defines the models for calculating stage signal and noise levels.

After iterative experiments with the analytical model and empirical verification with the RFG, the phase noise response in Figure 18 could be broken down into four regions (labeled A through D in the plot). The noise plateau in Region A is due to the noise contributions from the TMXO and all the circuitry through the 10-MHz comb generator to the input of the 100-MHz crystal filter. The noise roll-off in Region B is due to the noise bandwidth of the 100-MHz crystal filter. The noise plateau in Region C is due to (1) the level of the signal, relative to thermal noise, following the 100-MHz crystal filter, (2) phase noise enhancement in the 100-MHz comb generator, and (3) the signal level relative to thermal noise at the input of the amplifier that follows the 1-GHz filter. (Surprisingly, the additive noise contributed by the 100-MHz comb generator itself affects this region only slightly). The noise roll-off in Region D is due to the combined filtering of the 1- and 4-GHz filters. Beyond Region D, the roll-off to the thermal noise floor has negligible contribution to the total noise energy.



MEASUREMENT	TOTAL CNR (2S) 1 kHz TO 1 GHz (dBc)	PARTIAL CNR ±5 MHz, EXCL ±8 kHz (dBc)
RFG +20°C	-27.47	-35.26
ANALYSIS	-27.25	-35.76

Figure 18. RF Generator phase noise: measured vs. predicted.

TABLE 13(a) RFG Phase Noise Analysis

	B	C	D	E	F	G	H	I	J	K	L	M
2		TMXO	Level	cplr	Level	amp	Level	CMOS x10	Level	cplr & pad	Level	xtal bpf
3				TDC-10-2		A83-1				TDC-10-2&6dB		McCoy 20Q55
4		10 MHz	(dBm)	10 MHz	(dBm)	10 MHZ	(dBm)	100 MHz	(dBm)	100 MHz	(dBm)	100 MHz
5												
6	Nom gain (amb)			-2.00		20.00		-17.00		-8.00		-3.50
7												
8	Pout @ 1dB (nom)											
9	Pout @ sat (nom)					3.00		-14.00				
10												
11	NF (dB)			2.00		6.00				8.00		3.50
12	Noise floor (dBm/Hz)			-174.00		-174.00		-155.00		-174.00		-174.00
13	Noise enhancement (dB)							20.00				
14												
15	Ø Noise rej (dB)											
35	•••••••••••••••••	•••••	•••••	•••••••	•••••	•••••••	•••••	•••••••••	•••••	••••••• •••	•••••	•••••••••
36	Nominal signal level		-15.00		-17.00		3.00		-14.00		-22.00	
37												
38	Ø Noise (dBm/Hz @ fo)											
39	Lf (1e+3 Hz)		-155.00		-156.97		-136.96		-133.96		-141.96	
40	Lf (2e+3 Hz)		-155.00		-156.97		-136.96		-133.96		-141.96	
41	Lf (5e+3 Hz)		-155.00		-156.97		-136.96		-133.96		-141.96	
42	Lf (1e+4 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
43	Lf (2e+4 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
44	Lf (5e+4 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
45	Lf (1e+5 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
46	Lf (2e+5 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
47	Lf (5e+5 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
48	Lf (1e+6 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
49	Lf (2e+6 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
50	Lf (5e+6 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
51	Lf (1e+7 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
52	Lf (2e+7 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
53	Lf (5e+7 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
54	Lf (1e+8 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
55	Lf (2e+8 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
56	Lf (5e+8 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
57	Lf (1e+9 Hz)		-160.00		-161.90		-141.89		-138.89		-146.88	
58												
59	Øn (2S, 2 GHz) (dBm)		-67.00		-68.90		-48.89		-45.89		-53.88	
60	Øn (2S, 2 GHz) (dBc)		-52.00		-51.90		-51.89		-31.89		-31.88	

TABLE 13(b) RFG Phase Noise Analysis

	B	N	O	P	Q	R	S	T	U	V	W	X
2		Level	pad	Level	amp	Level	amp	Level	cplr	Level	GBL x10	Level
3					A86		A72		TDC-10-2			
4		(dBm)	100 MHz	(dBm)	100 MHz	(dBm)	100 MHz	(dBm)	100 MHz	(dBm)	1 GHz	(dBm)
5												
6	Nom gain (amb)		-3.00		28.00		13.50		-2.00		-28.00	
7												
8	Pout @ 1dB (nom)											
9	Pout @ sat (nom)				7.00		13.00				-17.00	
10												
11	NF (dB)		3.00		5.00		5.00		2.00			
12	Noise floor (dBm/Hz)		-174.00		-174.00		-174.00		-174.00		-155.00	
13	Noise enhancement (dB)										20.00	
14												
15	Ø Noise rej (dB)											
35												
36	Nominal signal level	-25.50		-28.50		-0.50		13.00		11.00		-17.00
37												
38	Ø Noise (dBm/Hz @ fo)											
39	Lf (1e+3 Hz)	-145.46		-148.45		-120.45		-106.95		-108.95		-116.95
40	Lf (2e+3 Hz)	-145.46		-148.45		-120.45		-106.95		-108.95		-116.95
41	Lf (5e+3 Hz)	-145.46		-148.45		-120.45		-106.95		-108.95		-116.95
42	Lf (1e+4 Hz)	-153.37		-156.33		-128.33		-114.83		-116.83		-124.83
43	Lf (2e+4 Hz)	-163.37		-166.00		-138.00		-124.50		-126.49		-134.49
44	Lf (5e+4 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
45	Lf (1e+5 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
46	Lf (2e+5 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
47	Lf (5e+5 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
48	Lf (1e+6 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
49	Lf (2e+6 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
50	Lf (5e+6 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
51	Lf (1e+7 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
52	Lf (2e+7 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
53	Lf (5e+7 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
54	Lf (1e+8 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
55	Lf (2e+8 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
56	Lf (5e+8 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
57	Lf (1e+9 Hz)	-174.00		-173.92		-145.90		-132.40		-134.40		-142.40
58												
59	Øn (2S, 2 GHz) (dBm)	-80.96		-80.90		-52.89		-39.39		-41.39		-49.39
60	Øn (2S, 2 GHz) (dBc)	-55.46		-52.40		-52.39		-52.39		-52.39		-32.39

TABLE 13(c) RFG Phase Noise Analysis

	B	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AI
2		cplr	Level	pad	Level	K&L BPF	Level	pad	Level	amp	Level	amp
3		(3) TDC-10-2		EMC		XB6PP1000/x60				A66-3		UTO-1058
4		1 GHz	(dBm)	1 GHz	(dBm)	1 GHz	(dBm)	1 GHz	(dBm)	1 GHz	(dBm)	1 GHz
5												
6	Nom gain (amb)	-16.00		-3.00		-4.50		-3.00		26.00		25.00
7												
8	Pout @ 1dB (nom)											
9	Pout @ sat (nom)									3.00		11.00
10												
11	NF (dB)	16.00		3.00		4.50		3.00		5.00		6.00
12	Noise floor (dBm/Hz)	-174.00		-174.00		-174.00		-174.00		-174.00		-174.00
13	Noise enhancement (dB)											
14												
15	Ø Noise rej (dB)											
35												
36	Nominal signal level		-33.00		-36.00		-40.50		-43.50		-17.50	
37												
38	Ø Noise (dBm/Hz @ fo)											
39	Lf (1e+3 Hz)		-132.95		-135.95		-140.45		-143.45		-117.45	
40	Lf (2e+3 Hz)		-132.95		-135.95		-140.45		-143.45		-117.45	
41	Lf (5e+3 Hz)		-132.95		-135.95		-140.45		-143.45		-117.45	
42	Lf (1e+4 Hz)		-140.83		-143.83		-148.32		-151.31		-125.31	
43	Lf (2e+4 Hz)		-150.48		-153.46		-157.88		-160.78		-134.77	
44	Lf (5e+4 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
45	Lf (1e+5 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
46	Lf (2e+5 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
47	Lf (5e+5 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
48	Lf (1e+6 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
49	Lf (2e+6 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
50	Lf (5e+6 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
51	Lf (1e+7 Hz)		-158.28		-161.16		-165.25		-167.69		-141.69	
52	Lf (2e+7 Hz)		-158.28		-161.16		-166.75		-168.98		-142.97	
53	Lf (5e+7 Hz)		-158.28		-161.16		-174.00		-173.92		-147.89	
54	Lf (1e+8 Hz)		-158.28		-161.16		-174.00		-173.92		-147.89	
55	Lf (2e+8 Hz)		-158.28		-161.16		-174.00		-173.92		-147.89	
56	Lf (5e+8 Hz)		-158.28		-161.16		-174.00		-173.92		-147.89	
57	Lf (1e+9 Hz)		-158.28		-161.16		-174.00		-173.92		-147.89	
58												
59	Øn (2S, 2 GHz) (dBm)		-65.27		-68.15		-80.20		-80.51		-54.48	
60	Øn (2S, 2 GHz) (dBc)		-32.27		-32.15		-39.70		-37.01		-36.98	

TABLE 13(d) RFG Phase Noise Analysis

	B	AJ	AK	AL	AM	AN	AO	AP	AQ	AR	AS	AT
2		Level	SRD x4	Level	µStrip BPF	Level	amp	Level	x2 mixer	Level	amp	Level
3							AMO-627-D		DMD18A07MK		(3) PPA 18632	
4		(dBm)	4 GHz	(dBm)	4 GHz	(dBm)	4 GHz	(dBm)	11 GHz	(dBm)	11 GHz	(dBm)
5												11GHz Output
6	Nom gain (amb)		-16.00		-1.50		22.00		-38.00		45.00	
7												
8	Pout @ 1dB (nom)											
9	Pout @ sat (nom)						10.00					
10												
11	NF (dB)		16.00		1.50		6.00				6.00	
12	Noise floor (dBm/Hz)		-155.00		-174.00		-174.00		-174.00		-174.00	
13	Noise enhancement (dB)		12.04						6.02			
14												
15	Ø Noise rej (dB)											
35												
36	Nominal signal level	7.50		-10.50		-12.00		10.00		-28.00		17.00
37												
38	Ø Noise (dBm/Hz @ fo)											
39	Lf (1e+3 Hz)	-92.45		-98.41		-99.91		-77.91		-109.89		-64.89
40	Lf (2e+3 Hz)	-92.45		-98.41		-99.91		-77.91		-109.89		-64.89
41	Lf (5e+3 Hz)	-92.45		-98.41		-99.91		-77.91		-109.89		-64.89
42	Lf (1e+4 Hz)	-100.31		-106.27		-107.77		-85.77		-117.74		-72.74
43	Lf (2e+4 Hz)	-109.77		-115.73		-117.23		-95.23		-127.21		-82.21
44	Lf (5e+4 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
45	Lf (1e+5 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
46	Lf (2e+5 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
47	Lf (5e+5 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
48	Lf (1e+6 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
49	Lf (2e+6 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
50	Lf (5e+6 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
51	Lf (1e+7 Hz)	-116.69		-122.65		-124.15		-102.15		-134.13		-89.13
52	Lf (2e+7 Hz)	-117.97		-123.93		-125.43		-103.43		-135.41		-90.41
53	Lf (5e+7 Hz)	-122.89		-128.85		-133.35		-111.35		-143.33		-98.33
54	Lf (1e+8 Hz)	-122.89		-128.85		-140.35		-118.35		-150.33		-105.33
55	Lf (2e+8 Hz)	-122.89		-128.85		-165.35		-143.34		-174.00		-129.00
56	Lf (5e+8 Hz)	-122.89		-128.85		-174.00		-151.92		-174.00		-129.00
57	Lf (1e+9 Hz)	-122.89		-128.85		-174.00		-151.92		-174.00		-129.00
58												
59	Øn (2S, 2 GHz) (dBm)	-29.48		-35.44		-45.28		-23.28		-55.25		-10.25
60	Øn (2S, 2 GHz) (dBc)	-36.98		-24.94		-33.28		-33.28		-27.25		-27.25

TABLE 13(e) RFG Phase Noise Analysis

	BK	BL	BM	BN	BO	BP	BQ
2	Filter Rej		xtal bpf		A-RF BPF		µStrip BPF
3							
4	@ Foffset (Hz)		100 MHz		1 GHz		4 GHz
5							
6			-3.50		-4.50		-1.50
7							
8							
9							
10							
11			3.50		4.50		1.50
12			-174.00		-174.00		-174.00
13							
14							
15							
16	1e+3		0.00		0.00		0.00
17	2e+3		0.00		0.00		0.00
18	5e+3		0.00		0.00		0.00
19	1e+4		-3.00		0.00		0.00
20	2e+4		-13.00		0.00		0.00
21	5e+4		-27.00		0.00		0.00
22	1e+5		-55.00		0.00		0.00
23	2e+5		-55.00		0.00		0.00
24	5e+5		-55.00		0.00		0.00
25	1e+6		-55.00		0.00		0.00
26	2e+6		-55.00		0.00		0.00
27	5e+6		-55.00		0.00		0.00
28	1e+7		-55.00		0.00		0.00
29	2e+7		-55.00		-1.50		0.00
30	5e+7		-55.00		-32.00		-3.00
31	1e+8		-55.00		-55.00		-10.00
32	2e+8		-55.00		-55.00		-35.00
33	5e+8		-55.00		-55.00		-50.00
34	1e+9		-55.00		-55.00		-50.00

TABLE 14

Component Parameter Models for Phase Noise Analysis

Parameter	Component	Model
Nominal gain (dB)	Amplifiers	Nominal linear gain of the amp or Psat-Pin; if Pin is above the amp's linear dynamic range
	Passive (pads, filters, etc.)	Nominal loss of the component
	Digital multipliers	Psat-Pin; if Pin is within the device's dynamic range
	SRD multipliers	Nominal loss; if Pin is within the device's dynamic range
Pout at sat (nom)	Amplifiers	Nominal saturated output power level
	Digital multipliers	Nominal output power level
NF (dB)	Amplifiers	Nominal device noise figure
	Passive (pads, filters, etc.)	Absolute value of its gain
Noise floor (dBm/Hz)	Multipliers	Estimated device noise floor based on published and empirical data
	All others	Thermal noise of resistor at 300°C
Noise enhancement (dB)	Multipliers	$20^{*}\log_{10}$(multiplication factor)
Ø Noise rejection (dB)	Filters	Noise rejection along filter skirt

TABLE 15

Signal and Noise Level Models for Phase Noise Analysis

Parameter	Component	Model
Nominal signal level (dBm)	All	Previous signal level + component gain
Ø Noise (dBm/Hz at f_o) Where f_o is offset frequency from carrier	Amplifiers, pads couplers	Previous noise level + gain + T_{eq}
	Filters	Previous noise level + gain + T_{eq}–filter rejection or –174, whichever is greater
	Multipliers	Previous noise level + noise enhancement + gain
Ø Noise (dBc/Hz at f_o)	All	Ø Noise (dBm/Hz at f_o) – signal level
$Ø_n$ (2S, 2 GHz) (dBm)	All	Ø Noise (dBm/Hz) integrated over 1 kHz to 1 GHz + 3 dB (double-sided noise)
$Ø_n$ (2S, 2 GHz) (dBc)	All	$Ø_n$ (2S, 2 GHz) (dBm) – signal level (double-sided noise)

6. IMPLEMENTATION DETAILS

6.1 TMXO MODULE

The tactical miniature crystal oscillator (TMXO) Module provides the 10-MHz reference to the RFG and is the frequency standard for the entire ASCAMP terminal. A block diagram of the TMXO Module is shown in Figure 19.

The TMXO is mounted in a socket on a small PC board to facilitate orientation within the module and to allow for replacement, if necessary. The TMXO has a small support board associated with it that allows for fine adjustment and setting of the output frequency. The TMXO is typically adjusted once during installation and then once per year. The adjustments are easily accessible once the top cover of the module has been removed. A schematic of the frequency set board connected to the TMXO is shown in Figure 20.

The TMXO Module also contains two additional PC boards for the 10-MHz comb generator and a +5-V linear regulator. The regulator provides line filtering, bias voltage regulation, and noise immunity for the 10-MHz comb generator board. This extra bias conditioning is needed because this circuitry has the most direct effect on phase noise at the RFG 11-GHz output, and the nominally available +5 V from the DC Converter System is shared with the "noisy" digital subsystems. A schematic of the +5-V regulator board is shown in Figure 21.

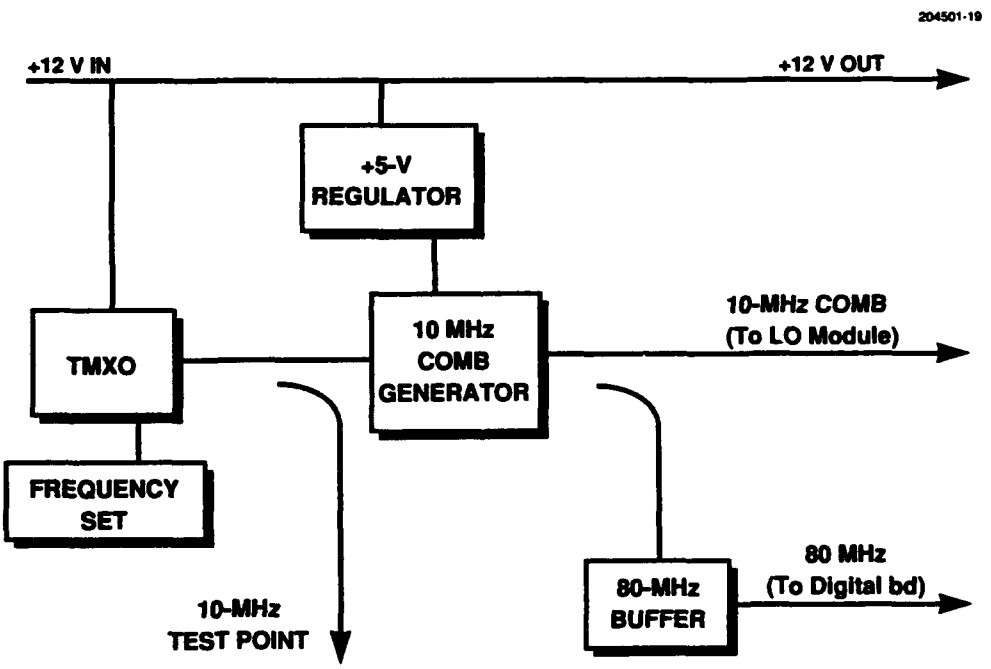


Figure 19. TMXO Module block diagram.

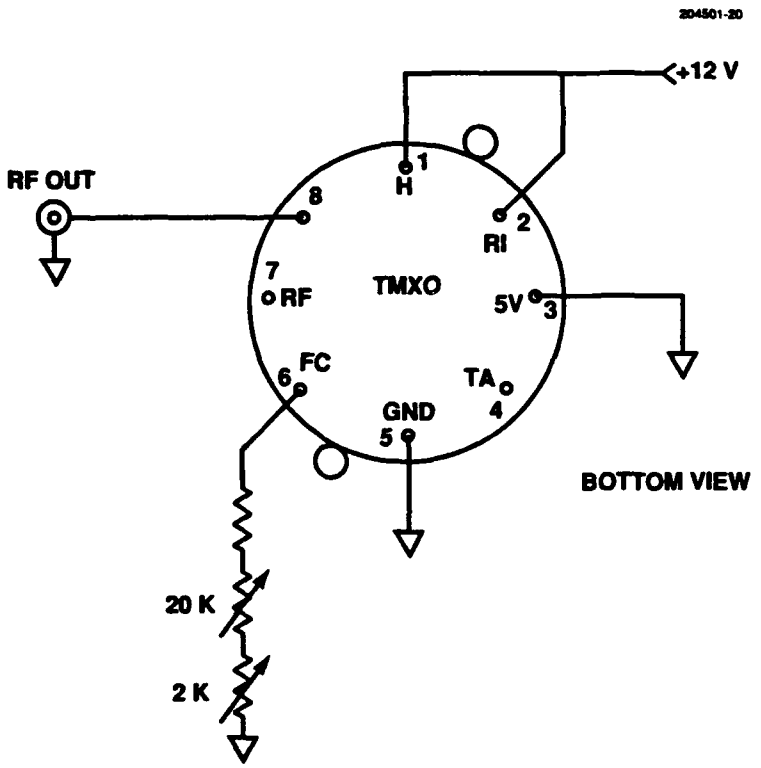


Figure 20. TMXO and frequency set schematic.

The 10-MHz comb generator board takes the sine-wave output from the TMXO (through a twisted pair connected to the TMXO mounting board) and the regulated +5 V. A portion of the 10-MHz signal is coupled off to provide an external 10-MHz test point and reference signal to phase lock external test equipment. The remaining circuitry generates a comb of harmonics based on the 10-MHz TMXO signal. A novel comb generator [9] was developed at Lincoln Laboratory in 1987, which uses digital devices to generate a set of harmonics. A pulse train, with a narrow pulse width and a repetition rate equal to the input frequency, is created by processing the 10-MHz signal with a series of digital gates. The Fourier transform of a pulse train in the time domain yields a set of harmonics in the frequency domain whose amplitudes roll off as $(\sin x)/x$. This process is the equivalent functionality of the more common comb generators implemented with varactors or step recovery diodes (SRDs). The advantage of this digital comb generator over the more common analog techniques is that it produces the required tones with much less dc power and does not require any tuning. The eighth harmonic is filtered and buffered to provide the required 80-MHz reference tone to the digital subsystems. The entire comb is sent to the 100-MHz reference board in the LO Module where it is filtered and used as the base frequency for the rest of the RFG. A complete schematic of the 10-MHz comb generator board is provided in Figure 22 and the output spectrum is shown in Figure 23.

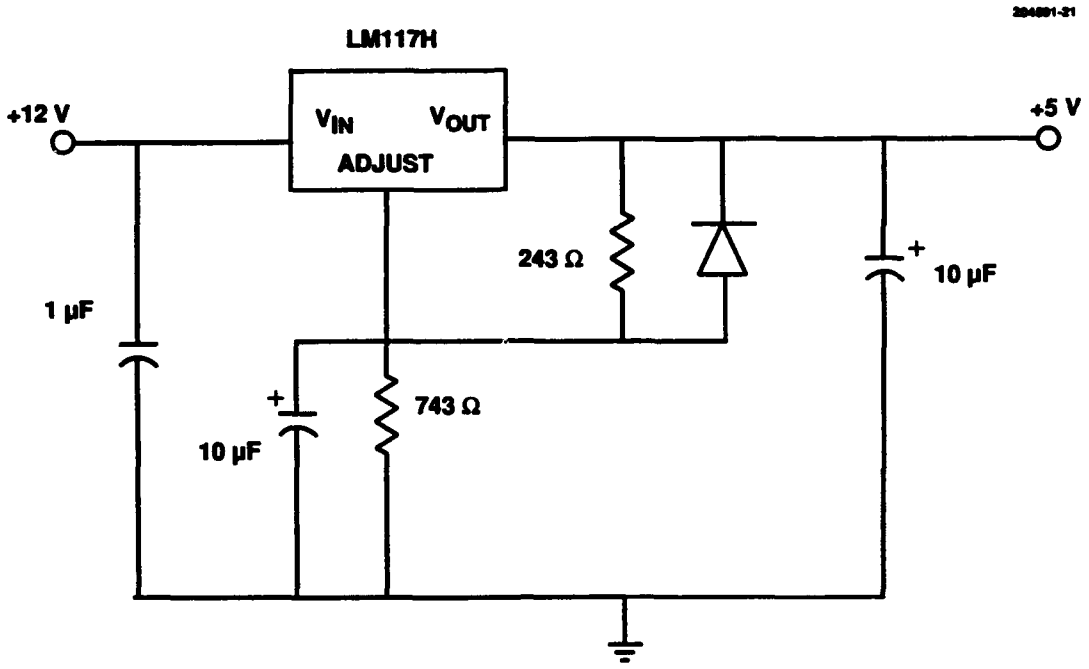


Figure 21. +5-V regulator board.

6.2 LO MODULE: FIXED FREQUENCY GENERATOR

The LO Module generates all the fixed frequencies that are required by the RFG. It takes the 10-MHz comb from the TMXO Module as its only rf input. The LO Module consists of five PC boards: the 100-MHz reference board, the 100-MHz comb generator board, the coupler board, the LO Board, and the SFB. The operating frequencies in this module range from 100 MHz to the 1.6-GHz output from the LO Board. Most of the PC boards in this module were fabricated on FR4 glass epoxy for low cost and mechanical strength. The exception is the LO Board, which was fabricated on Teflon laminated to an aluminum carrier.

6.2.1 100-MHz Reference Board

The 100-MHZ reference board filters and buffers the tenth harmonic from the 10-MHz comb generated in the TMXO Module. A 100-MHz crystal filter was used to ensure a very narrow noise bandwidth. The 20-kHz bandwidth of this filter sets one of the dominant phase noise pedestals in the RFG, which has a direct impact on total noise performance. A plot of the frequency response and noise bandwidth of this filter is shown in Figure 24. The crystal filter is followed by two buffer amplifiers that increase signal amplitude and provide isolation for the sensitive crystal filter from the remaining downstream circuitry, namely, the 100-MHz comb generator, a digital device. The second amplifier in this

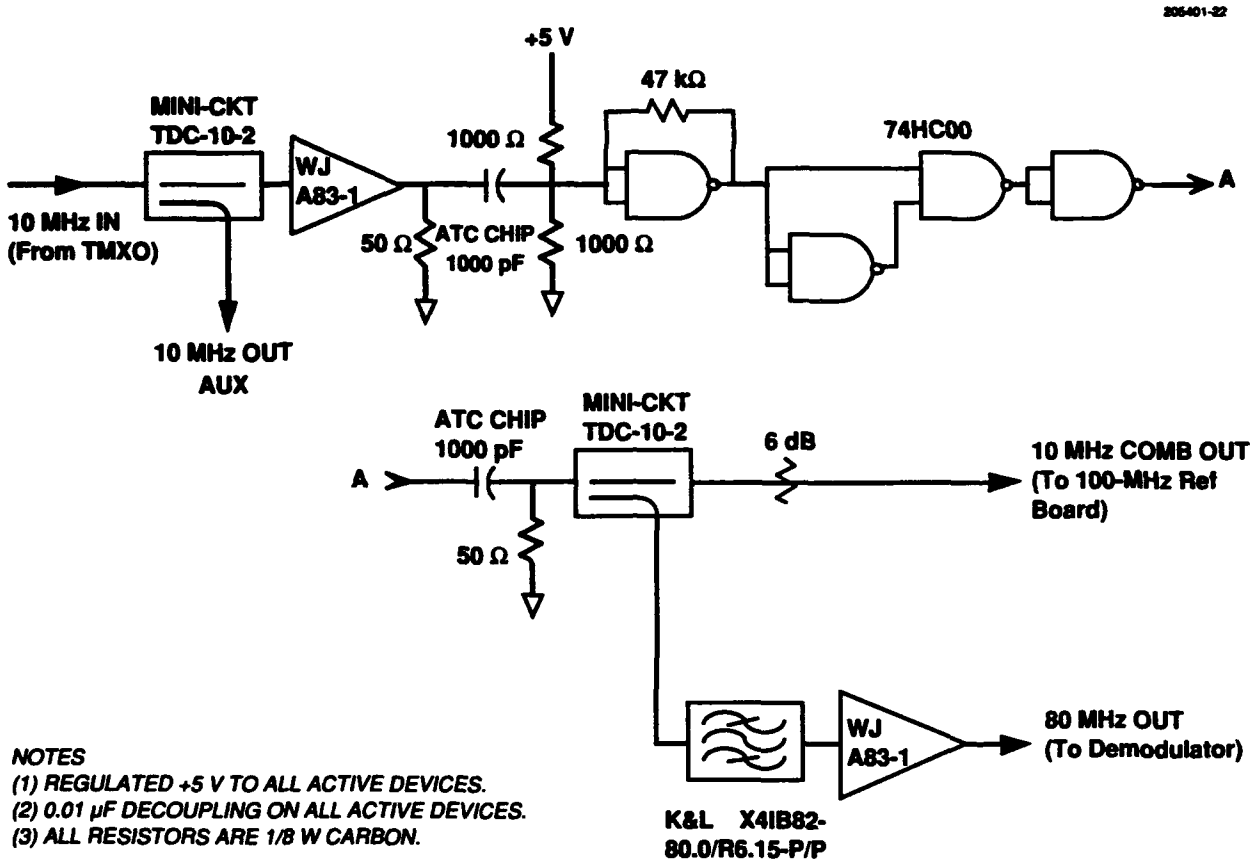


Figure 22. 10-MHz comb generator schematic.

cascade is driven into saturation to provide an acceptable level of temperature invariance in the output signal level. Also, the steep zero crossing of the limited waveform helps define a sharp transition for the digital comb generator that follows.

Additional bias line filtering was added to the dc feed of the on-board amplifiers. This filtering was necessary to reduce the amount of noise injected into the RFG from the switching dc converters. The converters have a typical switching frequency near 150 kHz, so a large value inductor and a capacitor were used to ensure adequate rejection.

The amplifiers are followed by a 10-dB coupler to extract the 100-MHz signal needed by the receiver. A simple low-pass filter was added to this coupled path to reduce the harmonic level sent to the receiver's second downconverter's LO port.

A schematic of the 100-MHz reference board is shown on Figure 25. This board was fabricated on a two-sided, FR4 epoxy PC board. Plated through holes provide low impedance rf ground to the top surface as well as providing a vertical, electrical shield through the PC board for extra rf isolation of the filtered 100 MHz.

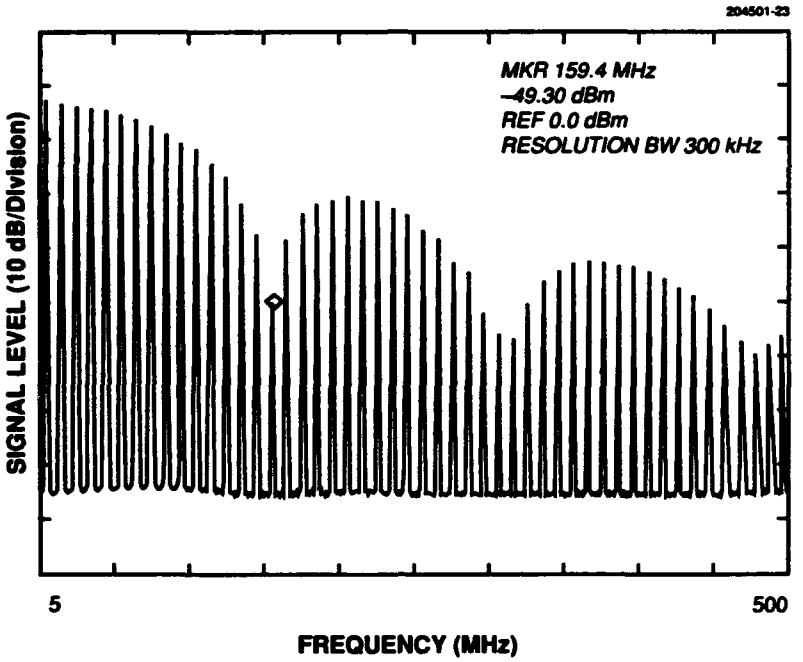


Figure 23. 10-MHz comb generator output spectrum.

6.2.2 100-MHz Comb Generator

The 100-MHz comb generator board takes the compressed 100-MHz signal from the 100-MHz reference board and produces a comb of harmonics with useful signals higher in frequency than the required 1000 MHz. Early on in the design phase, we decided to implement this circuit with the same digital technique used in the 10-MHz comb generator, which was described previously. In this circuit, the advantage of avoiding the more common SRD multiplier was even more pronounced. Because usable, stable output was required between the third and tenth harmonics, an SRD implementation would have required extensive tuning and a significant drive level in excess of what was available from low-power hybrid amplifiers. By implementing this circuitry with a digital technique, we achieved a spurious-free output spectrum that was adequately tolerant of temperature and input signal variations without any tuning or adjustments during the fabrication. The Giga-Bit Logic (GBL) GaAs components had the shortest propagation delays available, and their packaging and top surface vias allowed for bias decoupling and rf termination very close to the devices, which are critical in high-frequency digital applications. Three on-board, linear regulators generate the required voltages for the GBL device from the available ±5 V. A small shim under the GBL part provides for a low-impedance thermal path to the board metalization and additional low-impedance grounding.

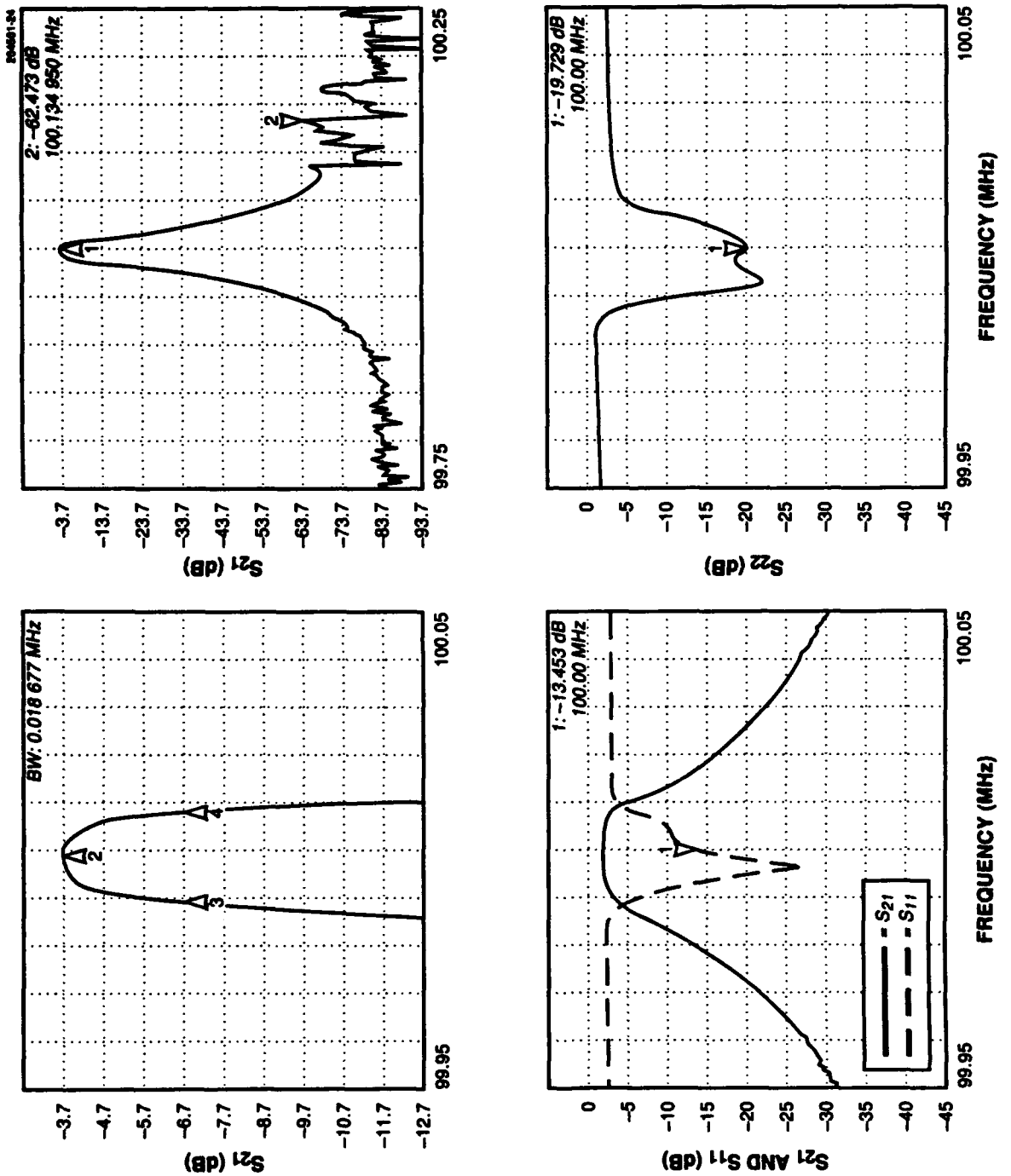


Figure 24. 100-MHz crystal filter frequency response.

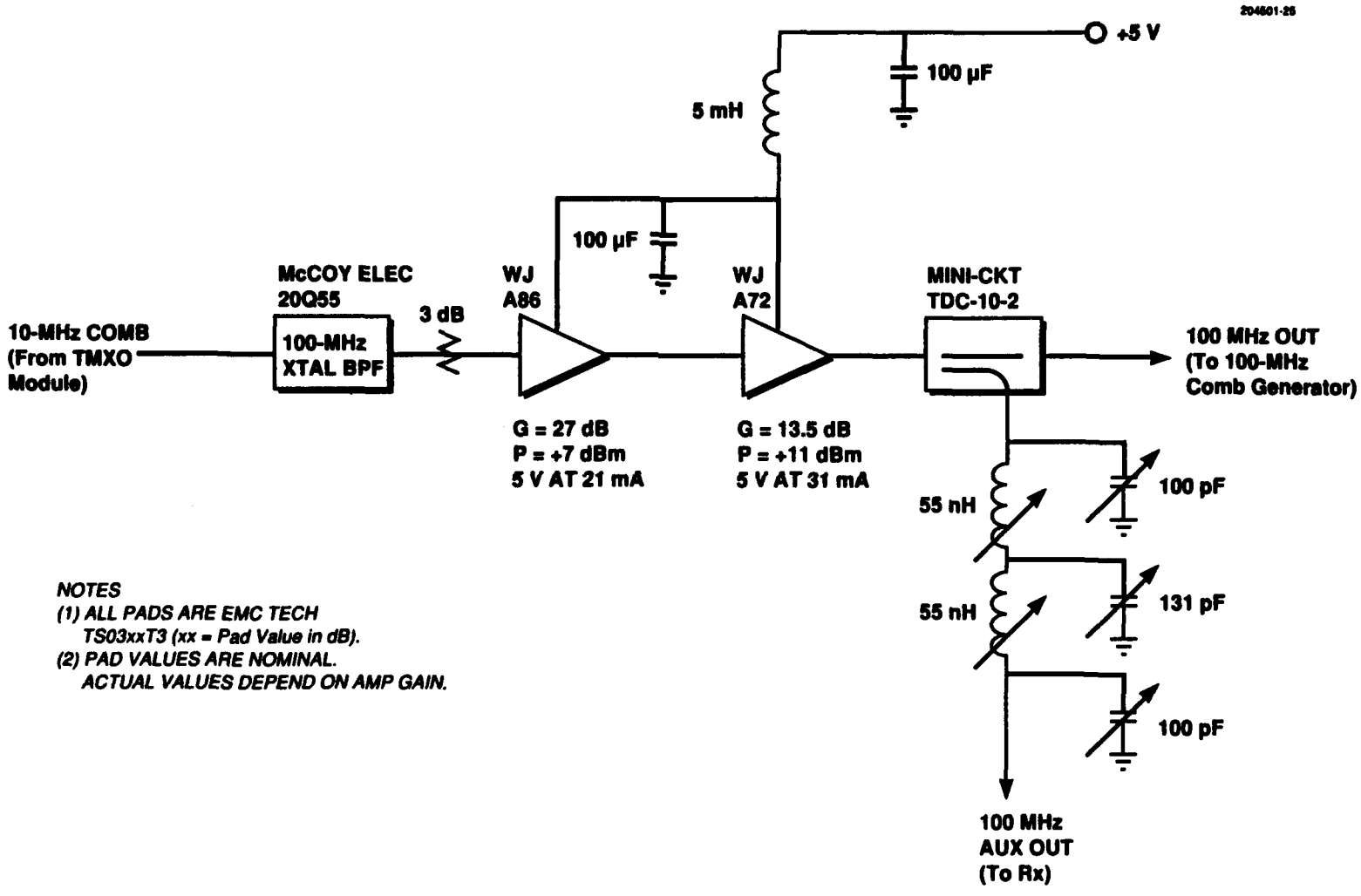


Figure 25. 100-MHz reference board schematic.

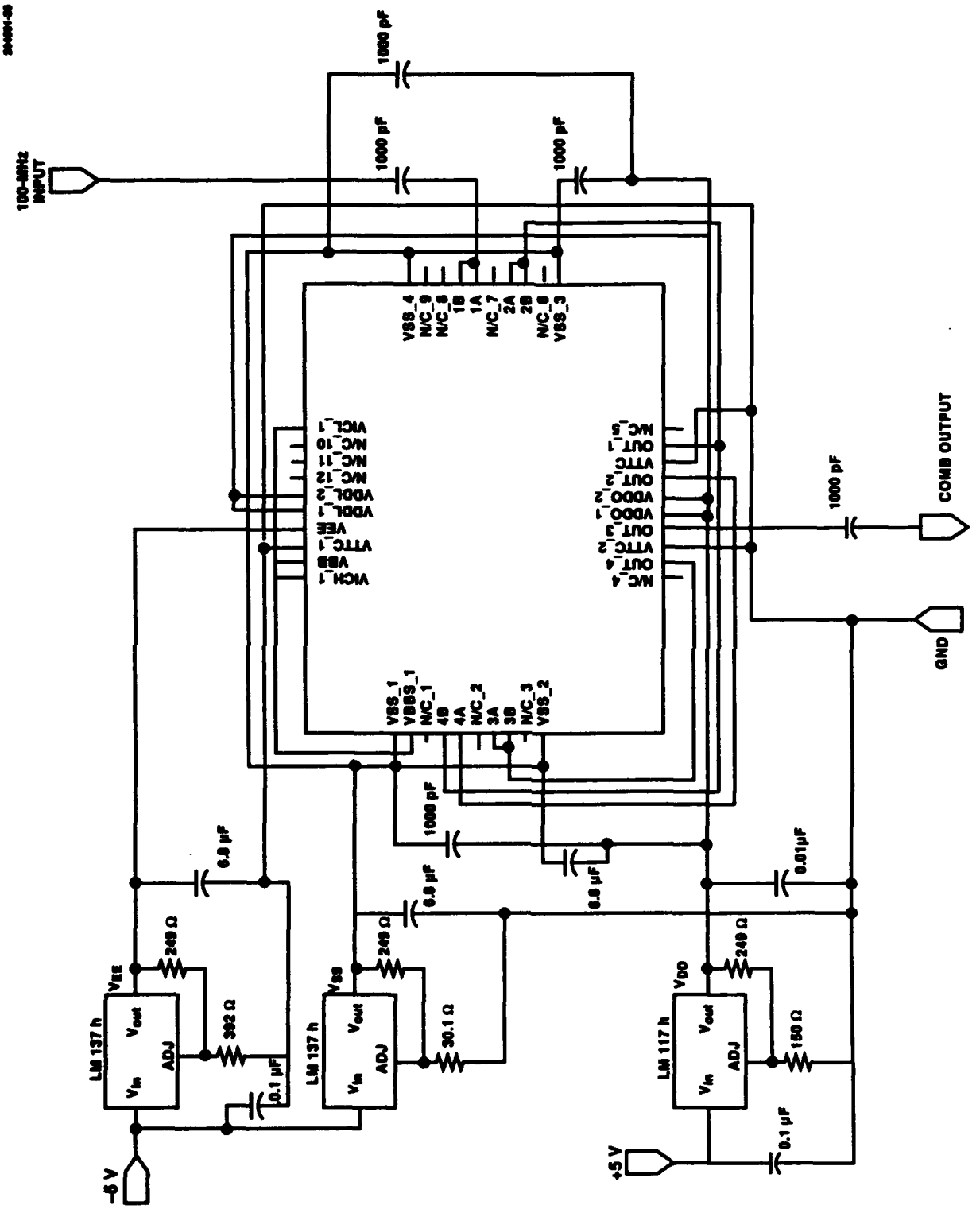


Figure 26. 100-MHz comb generator schematic.

A schematic of the 100-MHz comb generator board is shown on Figure 26. This board was built on a six-layer, glass epoxy board. This construction provided continuous ground and dc planes under the entire circuit. A plot showing the output spectrum is provided in Figure 27. The first null from the (sin x)/x shape can be seen at 1.5 GHz.

6.2.3 Coupler Board

The coupler board splits off the 100-MHz comb to the four signal paths that use it: the 300-MHz, the 1-GHz, the 800/1600-MHz paths, and the SFB, which uses the fifth through tenth harmonics. To provide isolation between the different signal paths, 10-dB couplers were used instead of power dividers. Mini-Circuits' couplers were chosen because of their small size and acceptable specifications. Unfortunately, they proved to have less directivity in our band than anticipated. Instead of taking the through port of the couplers to directly drive the SFB, an amplifier and two attenuators were added. This addition provided over 40 dB of reverse isolation between the fixed LO signals and the SFB, whose input impedance and return loss changes whenever a channel is switched. Improved performance with this extra isolation was most noticeable at the 1- and 1.6-GHz output. Because the 1000- and 800-MHz signals are used by both the SFB and the LO Board, variations of impedance and reflected signal level affected the LO Board output signal prior to adding the extra isolation. After adding the extra isolation components, the output level variation was adequate at less than 1 dB during channel switching.

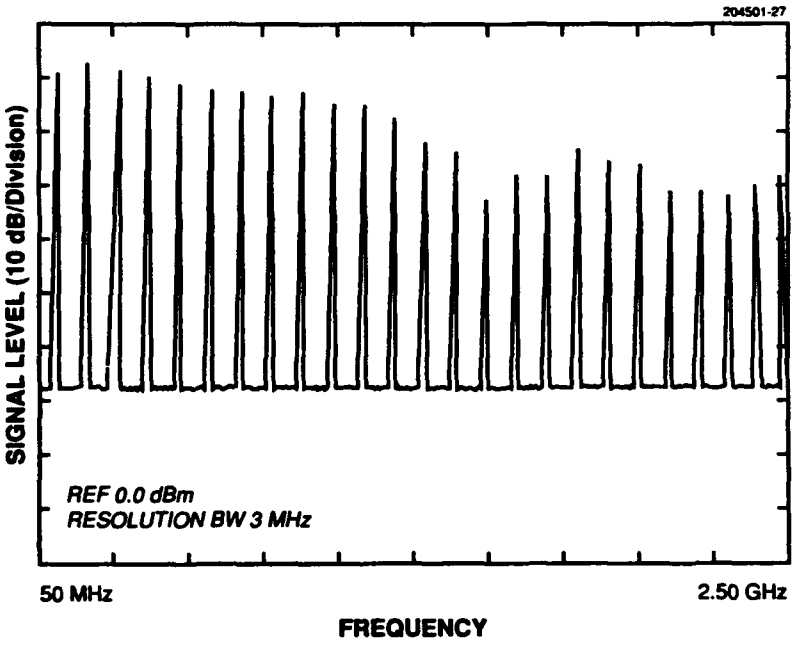
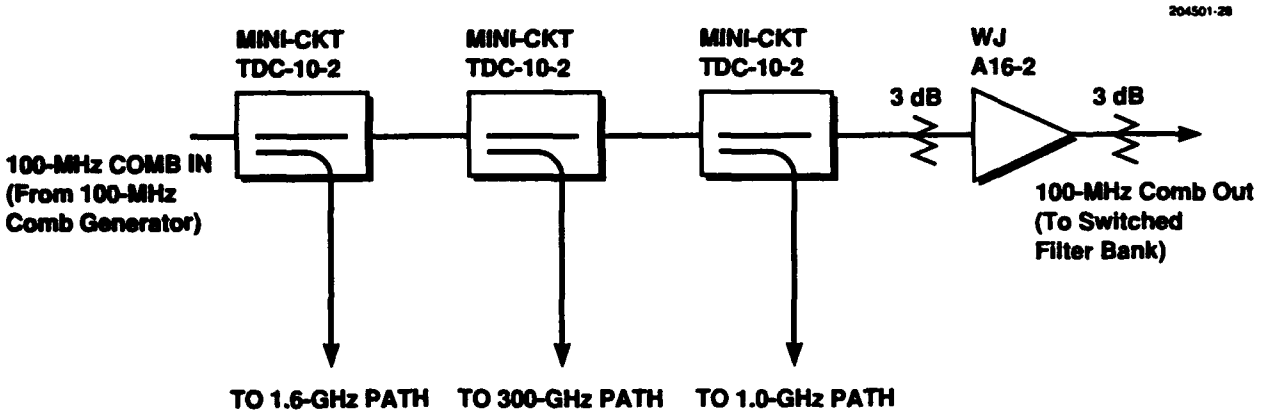


Figure 27. 100-MHz comb generator output spectrum.



NOTES
(1) +5 V TO ALL ACTIVE DEVICES.
(2) 0.01 μF DECOUPLING ON ALL ACTIVE DEVICES.
(3) ALL PADS ARE EMC TECH
TS03xxT3 (xx = Pad Value in dB).
(4) PAD VALUES ARE NOMINAL.
ACTUAL VALUES DEPEND ON AMP GAIN.

Figure 28. Coupler board schematic.

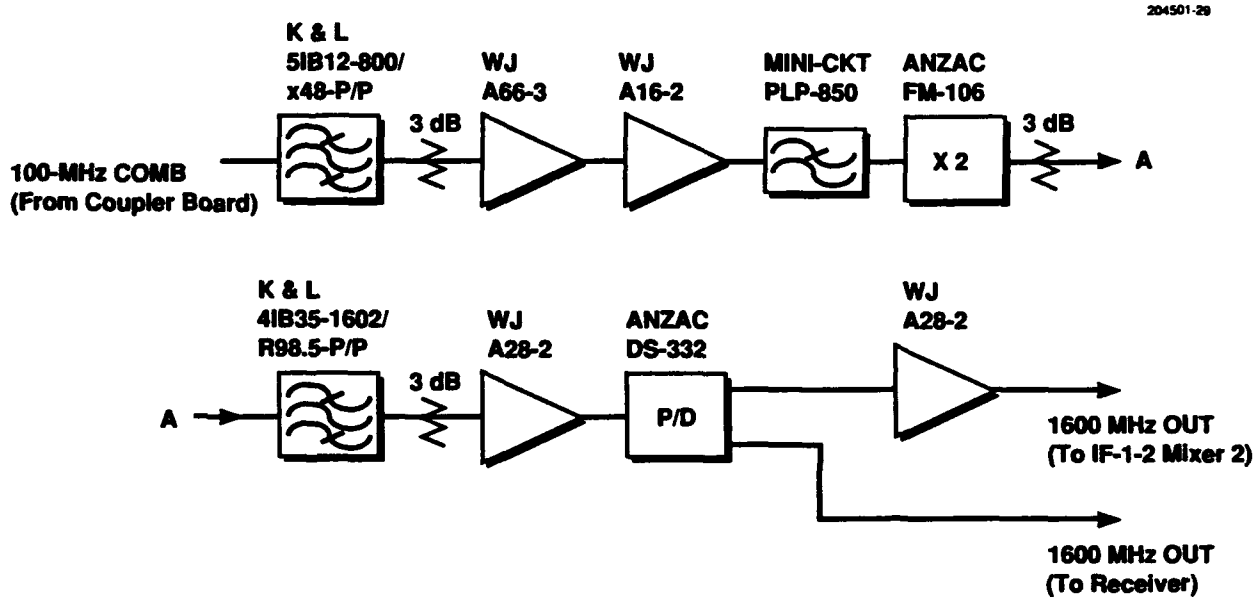
A schematic of the coupler board is shown on Figure 28. This board was fabricated on a two-sided, FR4 epoxy PC board.

6.2.4 LO Board

The LO Board contains three independent signal paths to generate fixed frequency outputs at 300, 1000, and 1600 MHz. This board was fabricated on a two-sided Duroid (Teflon) board that was soldered to a copper- and gold-plated aluminum carrier. This configuration allowed the milling away of superfluous Teflon board material between the different sections to increase rf isolation. The 0.020-in-thick Teflon substrate provided excellent 50Ω impedance lines at these frequencies. The 0.040-in-thick aluminum carrier provided mechanical rigidity and light weight, while the plating ensured good rf ground continuity without oxidation.

The output from the first coupler on the Coupler Board is fed to the 800/1600-MHz signal path. A schematic for the 1600-MHz path is shown in Figure 29(a). First, the 800-MHz tone is filtered off the comb, then amplified and doubled to 1600 MHz. The output of the doubler is then filtered to extract 1600 MHz, amplified, and split in a power divider. One branch of the power divider goes directly to the second

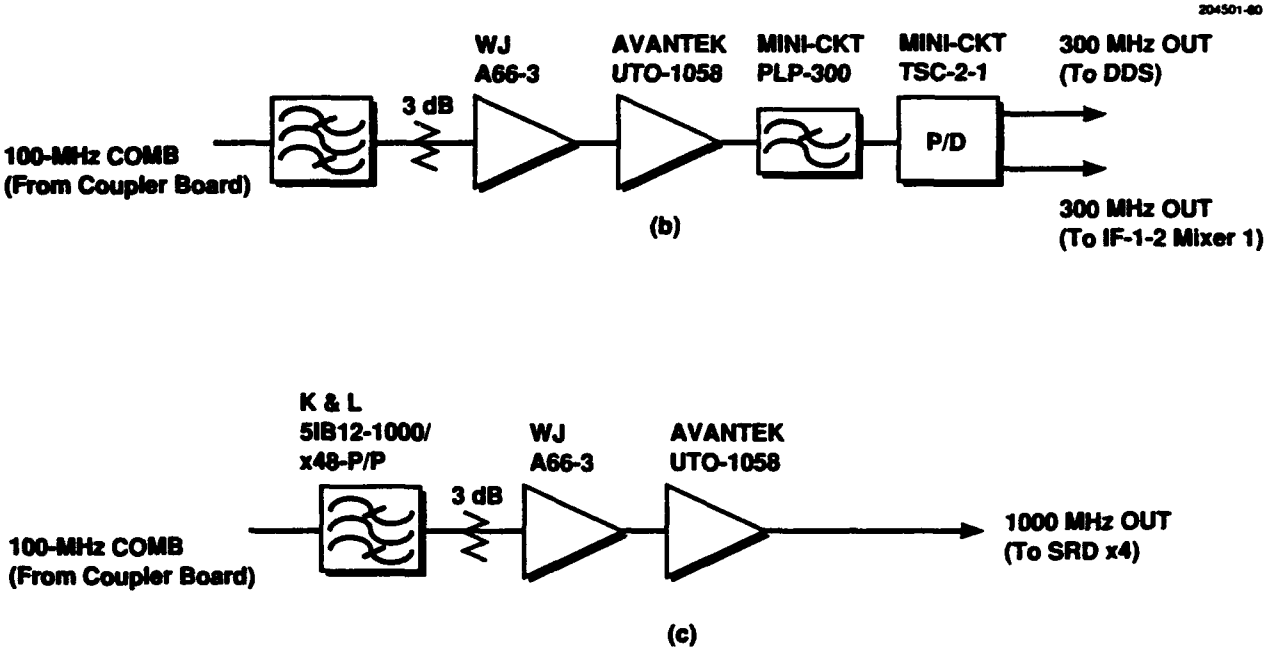
downconverter LO port of the receiver. The output power of 0 dBm ±2 dB is adequate for the receiver LO because it has an internal buffer/driver amp. The other branch of the power divider is amplified and then sent to mixer 2 on the IF-1-2 board in the RF Module. The 800-MHz band-pass filter was a custom-design component procured from K&L Microwave. It provided greater than 55-dB rejection of the adjacent ±100-MHz tones. The Mini-Circuits' 850-MHz low-pass filter preceding the doubler was used to decrease signal level of undesired harmonics from the frequency doubler's output. The 1600-MHz band-pass filter was a custom-design component procured from K&L Microwave. It provided greater than 55-dB rejection of the adjacent ±800-MHz tones. The stage gains and signal levels were designed so that the 800-MHz drive to the doubler and the 1600-MHz outputs levels are in compression (actually near saturation) to minimize signal level variation over temperature.



(a)

NOTES
(1) +5 V TO ALL AMPS.
(2) 0.01 μF DECOUPLING ON ALL AMPS.
(3) ALL PADS ARE EMC TECH
TS03xxT3 (xx = Pad Value in dB).
(4) PAD VALUES ARE NOMINAL.
ACTUAL VALUES DEPEND ON AMP GAIN.

Figure 29. (a) LO Board: 1600-MHz path schematic.



NOTES
(1) +5 V TO ALL AMPS.
(2) 0.01 μF DECOUPLING ON ALL AMPS.
(3) ALL PADS ARE EMC TECH
TS03xxT3 (xx = Pad Value in dB).
(4) PAD VALUES ARE NOMINAL.
ACTUAL VALUES DEPEND ON AMP GAIN.

Figure 29. (b) LO Board: 300-MHz path schematic and (c) LO Board: 1000-MHz path schematic.

The output from the second port of the coupler board is fed to the 300-MHz signal path. A schematic for the 300-MHz path is shown in Figure 29(b). The 300-MHz tone is filtered off from the comb; then it is amplified, filtered, and split by a power divider. One branch of the power divider drives the clock driver circuit on the DDS board in the RF Module. The other branch of the power divider drives the LO port of mixer 1 in the IF-1-2 board in the RF Module. The stage gains and signal levels were designed so that the 300-MHz output levels were in compression (actually near saturation) to minimize signal level variation over temperature. The 300-MHz band-pass filter was a custom-design component, procured from K&L Microwave, which provided greater than 55-dB rejection of the adjacent ±100-MHz tones. The 300-MHz low-pass filter attenuates the harmonics from the compressed amplifier to help reduce spurs in mixer 1 of the IF-1-2 board. The Mini-Circuits' low-pass filter was chosen for its small size and low cost. Although it was designed with an f_c of 300 MHz, the band edge attenuation still allows for adequate signal level at the two output ports.

The third port on the coupler board is fed to the 1000-MHz signal path [a schematic is provided in Figure 29(c)]. The 1000-MHz tone is filtered from the comb of harmonics and then amplified. The output from this stage is used to drive the SRD times-4 multiplier in the RF Module. The stage gains and signal levels were designed so that the 1000-MHz output level was in compression (actually near saturation) to minimize signal level variation over temperature. The 1000-MHz band-pass filter was a custom-design component, procured from K&L Microwave. It provided greater than 55-dB rejection of the adjacent ±100 MHz-tones. This filter also sets the 30-MHz band edge for one of the RFG noise pedestals, as discussed in Section 5.4. This noise bandwidth is a critical factor in the total noise of the RFG. Although the noise floor here is very low, the large bandwidth over which the total noise is integrated results in this pedestal being a major contributor to the total noise power. (By substituting a narrower band filter in place of the one currently in use, the total RFG phase noise could be directly reduced. This is discussed in Section 8.) Extra shielding was added to this section of the LO Board to minimize radiant coupling of 10-MHz sidebands to the 1-GHz output. A custom-formed metal shim was used for the shielding. It was grounded directly to the aluminum carrier and covered the entire 1-GHz section. This shielding was necessary due to the high sideband enhancement factor from the following stages of frequency multiplication.

6.2.5 Switched Filter Bank

A block diagram of the switched filter bank (SFB) is shown in Figure 30(a). The SFB takes the entire 100-MHz comb from the through port of the coupler board. The filter bank selectively passes one of the harmonics between 500 and 1000 MHz and rejects the rest. A pair of single-pole, six-throw switches route the comb through the desired band-pass filter. All of the band-pass filters were custom-design components, which were procured from K&L Microwave and provided greater than 55-dB rejection of the adjacent ±100-MHz tones. A set of attenuators, one per channel, precedes the second switch and allows for "select-in-test" signal level adjustment to compensate for unequal harmonic levels and variations between the insertion loss of the different filters. The selected tone is then amplified and output to the IF port of mixer 3 on the IF-1-2 board in the RF Module.

A pair of switches was chosen as the method of routing the signal through the filter bank, instead of a single switch and a six-way power divider combination, to reduce the amount of signal loss and eliminate an additional gain stage [12]. Also, having two switches allowed for a relaxation of the isolation requirement for the switches. This was very important because the compact layout of the hybrid switch made high channel-to-channel isolation difficult.

The hybrid switches [13] were designed and built at Lincoln Laboratory. This custom design was required because of the unavailability of commercial six-throw switches at these frequencies. The switch design was implemented by tying the input of six GaAs FET MMIC single-pole, single-throw switches to a common port. When one switch is turned on, the others are all in the off state. The common port was designed with a low-pass matching network to absorb the parasitic capacitance of the switches in the off state. This matching design extended the useful bandwidth of the switch network beyond the required 1 GHz. Because the switch is implemented with GaAs FETs, only a change in gate voltage is required to make the switch change state. The design of the MMIC's bias network used a floating circuit to make the switches TTL-controllable without additional level shifting circuitry. A schematic of a single MMIC

switch with its bias network is shown in Figure 30(b). The drive circuitry was built into the hybrid with high-speed CMOS devices to minimize power consumption. A photograph of the switch hybrid is shown in Figure 31.

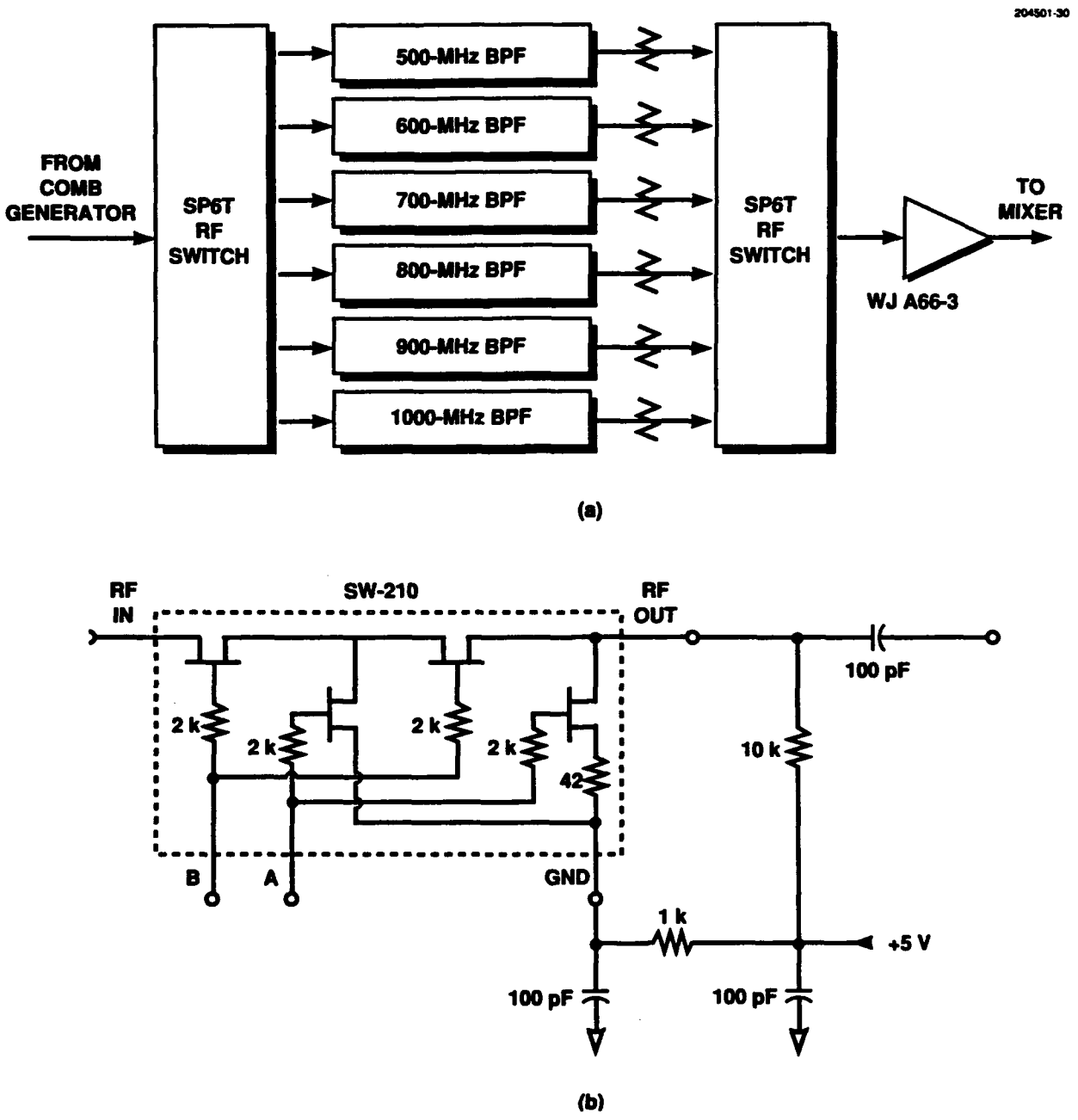


Figure 30. (a) Switched Filter Bank block diagram and (b) schematic of a SPST GaAs FET MMIC with bias network.

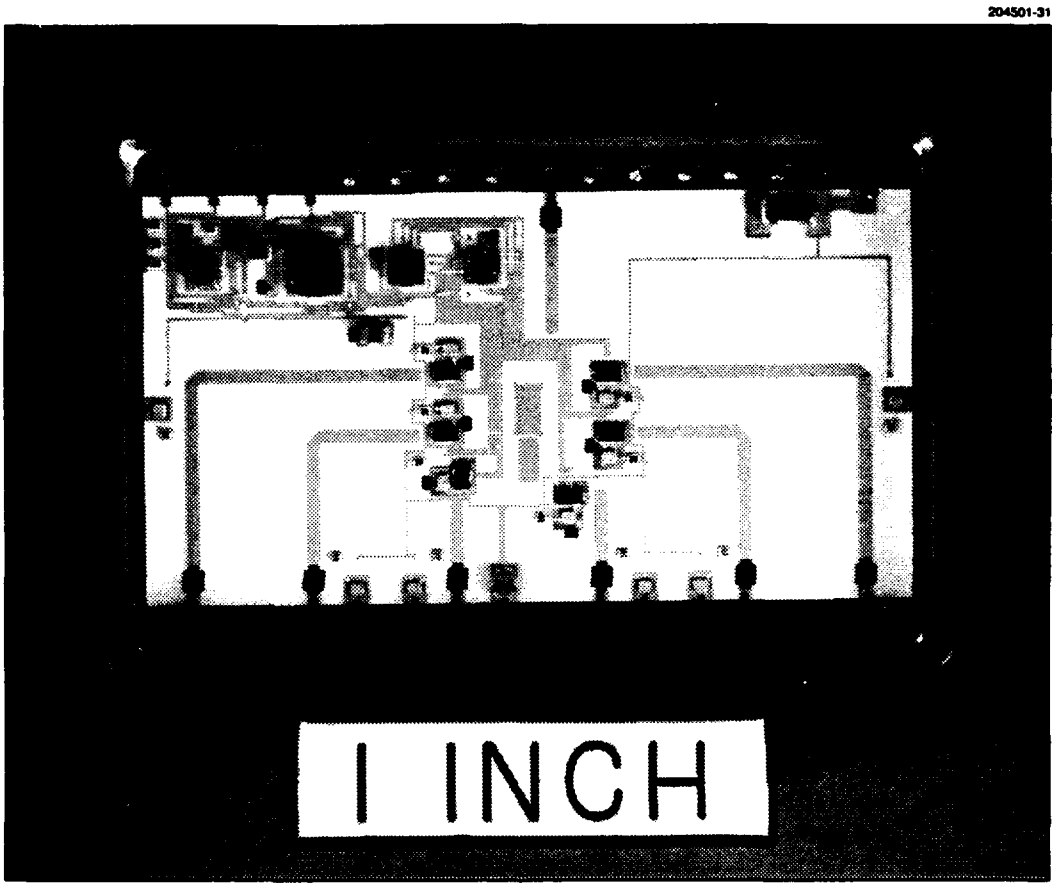


Figure 31. Photograph of SP6T switch hybrid.

6.3 RF MODULE: RF SIGNAL PATH

The RF Module generates the hopping output that is used to drive the transmitter and first downconversion stage's LO port in the receiver. The synthesizer's hopping signal path starts on the DDS board, which generates 50 MHz of tuning bandwidth. This frequency band is upconverted, doubled, and expanded in the IF-1-2 board to a 600-MHz band centered at 3.1 GHz. The remaining stages of the RF Module perform the final upconversion to 11 GHz, filtering, and amplification of the signal to its +12-dBm output. This module also contains an SRD times-4 multiplier to generate the 4-GHz LO signal for the final stage's harmonic mixer.

The RF Module contains a wide variety of board and component types due to the different operating frequencies and functions of the PC boards. The DDS board has digital frequency commands that are clocked at 2 MHz with repetition rates less than 20 kHz. Fixed frequency LOs that come from the

LO Module are between 300 and 1600 MHz, and the final output is at 11 GHz. The components in the RF Module range from digital and analog ICs, ASICs, and a programmable gate array to rf and microwave hybrids and packaged MMIC components as well as the usual assortment of capacitors, resistors, and chip attenuators. This mix of frequencies and technologies resulted in the RF Module containing one two-layer, FR4 epoxy board (+9-V linear regulator); one six-layer, FR4 epoxy board (DDS); one two-sided Duroid Teflon board on an aluminum carrier (IF-1-2 board); and 12 ceramic substrates on Kovar carriers (high-frequency section).

6.3.1 DDS Board

The DDS board is the heart of the synthesizer portion of the RFG. It takes a 300-MHz clock from the LO Board in the LO Module and digital frequency commands from the Keystream Processor (KP) in the digital subsystem to generate a hopping carrier between 50 and 100 MHz. The PC board was fabricated with a six-layer, FR4 epoxy. The schematic is shown in Figure 32.

The DDS with the highest clock rate that was available at the time of the synthesizer design was based on the STEL-2172 numerically controlled oscillator (NCO) made by Stanford Telecommunications. It has a 28-bit parallel input word and runs at clock rates up to 300 MHz. This integrated circuit has N=28, M=8, and L=8 internal data structures for the sine-wave computation. The 28 phase accumulator inputs are TTL levels, but the outputs are ECL levels. The chip dissipates about 7 W because the heart of the chip is ECL, a power-hungry technology.

Clocking the DDS at only 240 MHz would have made the frequency computations in the KP relatively simple due to the numerology. This could have provided 50 MHz of usable tuning range. Clocking the DDS at 300 MHz added a double-precision multiply to the frequency calculations; however, this did not have a major impact on the load of the KP. Choosing a clock rate of 300 MHz reduces the amount of hardware required to generate the clock (being a multiple of 100 MHz and directly available from the 100-MHz comb generator board in the LO Module). This design reduces dc power consumption by ~ 1 W, which is what would have been needed for a divider to generate 240 MHz. Although a 300-MHz DDS could potentially provide 100 MHz of usable tuning range, the 50-MHz bandwidth was maintained to allow for the possibility of implementing an alternative high-speed CMOS DDS that was under development at Lincoln Laboratory. Unfortunately, that technology, which would have significantly reduced dc power consumption, was unable to achieve clock rates, over temperature, sufficient for 50 MHz of tuning range.

The STEL NCO takes the frequency command word and generates an 8-bit amplitude quantized representation of a sine wave at the correct frequency. The 8-bit word is fed to a Honeywell HDAC51400 ECL DAC that generates a staircase approximation of a sine wave. After low-pass filtering on the IF-1-2 board, the result is a sinusoid that conforms to the following equation.

$$f_{DDS} = \frac{\text{Increment} * f_{clock}}{2^N}$$

$$= \text{frq cmd} * \frac{300\ \text{MHz}}{2^{28}} \quad . \tag{13}$$

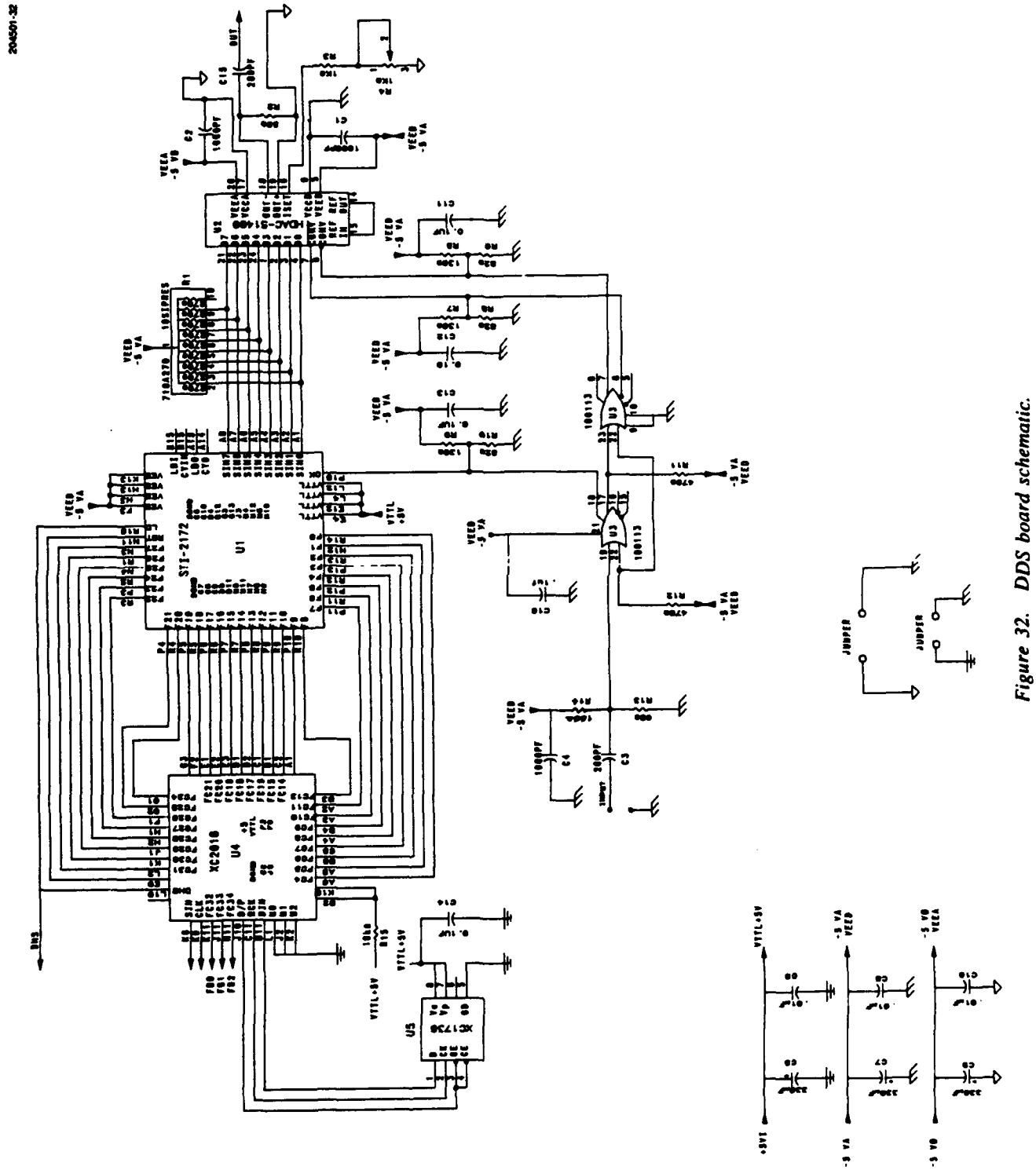


Figure 32. DDS board schematic.

The spurious performance of this design is typical of a commercial grade 8-bit DDS. Worst-case single spurs across the tuning range are typically –42 to –39 dBc and are primarily caused by amplitude quantization and glitch noise in the DAC. This results in many in-band spurs that are fold-overs from high-frequency products of the sampled digital system. The spurious content of the DDS output varies greatly across the tuning range with some frequencies having no spurs at all, some with many low level spurs, and others with a few discrete high-level spurs of –42 dBc. Because the ASCAMP terminal is a spread spectrum communications system, the statistical nature of the spurs is a more valid measure of performance than a single worst-case number. The spurious performance of the entire RFG is detailed in Section 7.3.

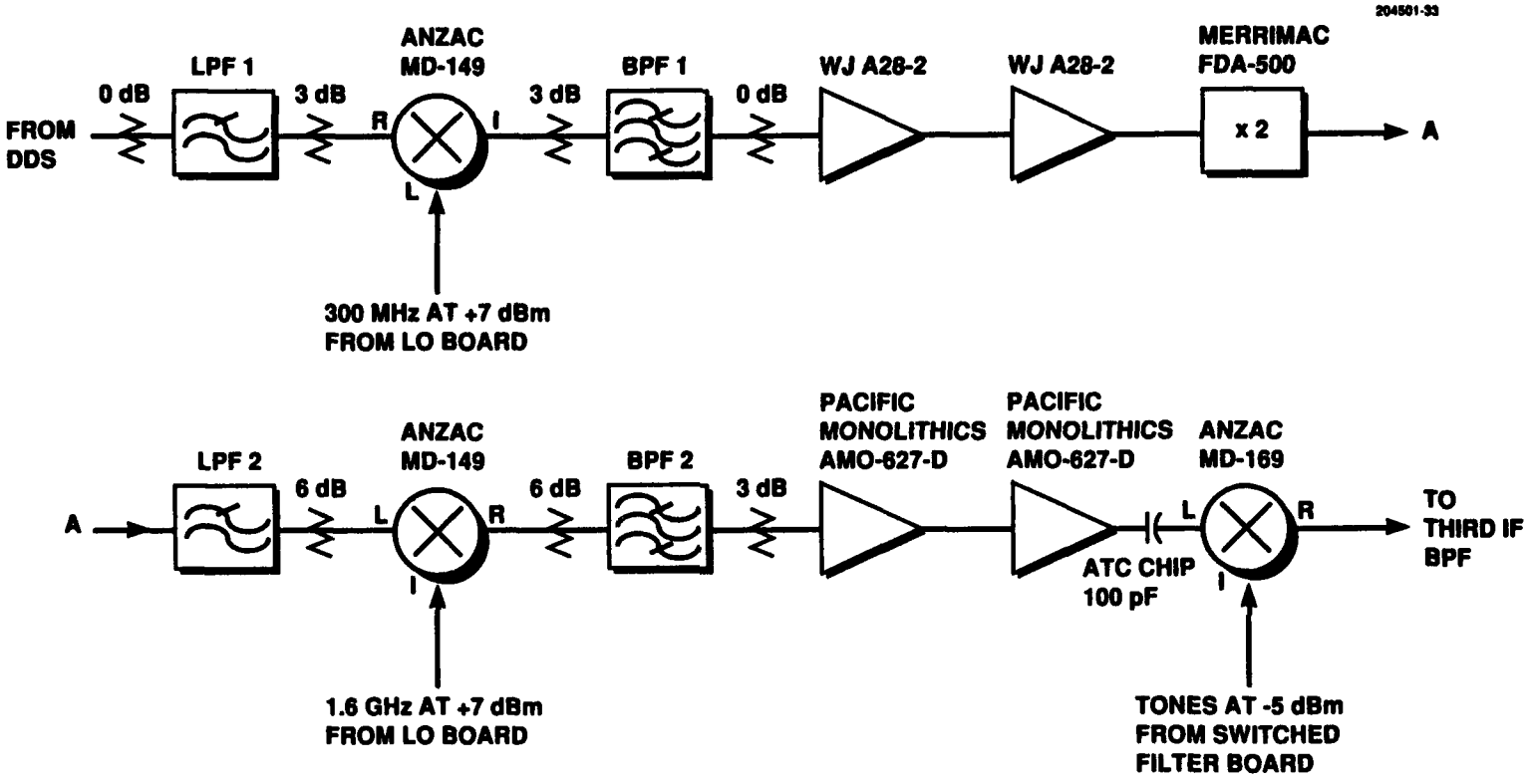
The digital frequency command arrives on three serial lines: hop sync, which signals a new frequency; data clock, which clocks the serial data into the Xilinx gate array; and serial data, which contains the 31-bit frequency command. (The command word format and frequency commands are described in more detail in Section 5.2.) The Xilinx programmable gate array transforms the serial command stream into a parallel word as well as strips off and routes the 3-bit command word for the SFB, which selects the appropriate channel for bandwidth expansion. The Xilinx part is automatically programmed at power-on by an on-board ROM. This method allows for easy testing and modification of the Xilinx functionality but leads to a potential turn-on sequencing situation.

The 300-MHz signal comes from the LO Board in the LO Module and is buffered by a ECL 100F series clock driver before being routed to the NCO and DAC. The entire DDS board takes 9.7 W of dc power. The primary heat sources are the NCO and DAC. A standard heatsink mounted to the top of the DAC provides sufficient radiant thermal transfer to the module cover to maintain the device well below its maximum junction temperature. A custom heatsink with integral stress relief was designed for the NCO to provide a direct, conductive thermal path from the top surface of the NCO to the chassis wall. The chassis wall was thickened in that area. A mounting screw directly under that wall allows for a low-thermal resistance path from the NCO to the chassis wall to the ASCAMP terminal structure.

6.3.2 IF-1-2 Board

The IF-1-2 board contains three upconversion stages and one frequency doubler. It takes the 50- to 100-MHz tuning range from the DDS board and expands the bandwidth to 600 MHz while shifting the frequency range to an output of 2.8 to 3.4 GHz. Besides the DDS, its inputs are a fixed frequency 300 MHz from the LO Board in the LO Module, a fixed frequency 1600 MHz from the LO Board in the LO Module, and a selectable, single tone of 500, 600, 700, 800, 900, or 1000 MHz from the SFB in the LO Module. It uses +5- and +9-V bias lines. A schematic is shown in Figure 33.

This board was fabricated on a two-sided Duroid (Teflon) board that was soldered to a copper- and gold-plated aluminum carrier. This configuration allowed the milling away of superfluous Teflon board material between the different IF sections to increase rf isolation. The 0.010-in-thick Teflon substrate provided excellent 50Ω impedance lines at these frequencies and closely matched the line width on the ceramic 3-GHz band-pass filter that follows mixer 3. The 0.050-in-thick aluminum carrier provided mechanical rigidity and light weight, while the plating ensured good rf ground continuity without oxidation. The Duroid was milled out between the input and output pins of the two band-pass filters, down



NOTES
(1) +5 V TO ALL WJ AMPS.
(2) +9 V TO ALL PM AMPS.
(3) 0.01 µF DECOUPLING ON ALL AMPS.
(4) PORTS ARE REVERSED ON MIXER 2 TO REDUCE SPURS.
(5) ALL PADS ARE EMC TECH TS03xxT3 (xx = Pad Value in dB).
(6) PAD VALUES ARE NOMINAL. ACTUAL VALUES DEPEND ON AMP GAIN.

FILTER PART NUMBERS
LPF 1: K&L 4IL81 - 112/R1116-P/P
LPF 2: MINI-CKT PLP-850
BPF 1: K&L 5IB22-376/R56.3-P/P
BPF 2: K&L 4IB35-2353/R137-P/P

Figure 33. IF-1-2 board schematic.

the length of the board to improve isolation between the parallel sections, and under the three mixers to allow them to be mounted directly to the metal carrier for improved grounding. The aluminum carrier is thicker under the two Pacific Monolithic amplifiers that drive the LO port of mixer 3. This extra thickness allowed for milling a well into the carrier so these amps, which are considerably thicker than the mixers, could be mounted directly to the metal carrier for good grounding. After assembly into the RF Module chassis, an aluminum divider wall slides into groves in the chassis to improve isolation between the parallel signal paths on the board. The divider wall makes contact with the chassis walls and cover and the board's metal carrier with a "Spira-Shield" compressive, metal gasket. The module chassis itself has an almost continuous, narrow ledge under the perimeter of the IF-1-2 board to ensure adequate grounding without adding excessive metal and weight.

The 50- to 100-MHz tuning range from the DDS board is first put through a low-pass filter with a 112-MHz cut-off frequency to reject the DDS's alias terms, clock leakage, and high-frequency spectral components. The resulting sine wave is upconverted in mixer 1 whose 300-MHz LO originates in the LO Board in the LO Module. The 350- to 400-MHz band output of this mixer is band-pass filtered in a custom-design component that was procured from K&L Microwave. This filter rejects the mixer's LO leakage, lower sideband, and other mixer spurs (Manley-Rowe products). This filter also rejects DDS-generated spurious outside the tuning range. This has a significant impact when the total noise power at the RFG output is measured by adding the energy from all spurious components of a carrier signal. Because the (2, 1) spur is at the band edge and cannot be adequately filtered, the mixer's input signal level from the low-frequency path was adjusted to ensure the spur amplitudes would be adequately small.

The signal is then boosted by a cascade of two hybrid amps to generate sufficient amplitude to drive the subsequent frequency doubler. The second amplifier in this chain is driven slightly into compression to reduce signal level variation over temperature. The frequency doubler both converts the band to a higher frequency range and expands the tuning range to a 700- to 800-MHz band. This is the only frequency multiplier stage in the hopping signal path of the RFG. This was an important trade-off between phase noise and spurious enhancement from multipliers versus other methods to expand the narrow tuning bandwidth available from the DDS. The output of the doubler is filtered by only a small low-pass filter. By not using a band-pass filter, a smaller sized low-pass filter could be used. However, this filter could not be eliminated altogether because the higher order terms from the doubler would cause excessive spurs in the subsequent mixer stage. Filtering of the doubler's fundamental feed through was accomplished in the next band-pass filter.

The hopping signal is then frequency shifted by mixer 2 to an output band of 2.3 to 2.4 GHz. As was explained in Section 5.3.2, this mixer is connected in a nonstandard way to eliminate the problem of the (–1, 2) Manley-Rowe product falling in-band. The low-level 700- to 800-MHz signal from the doubler is connected to the mixer's LO port. The high-level 1600-MHz driver signal from the LO Board in the LO Module is connected to the mixer's IF port, and the 2.3- to 2.4-GHz output is extracted from the mixer's RF port. This connection topology takes advantage of the balance of the internal balun/coupler network of the mixer's LO port to null out the (–1, 2) term. The spurs that are no longer suppressed, due to the port reversal, are far out-of-band and easily filtered. The output of mixer 2 is then

band-pass filtered in a custom-design component procured from K&L Microwave. This filter rejects the mixer's LO leakage, lower sideband, and other out-of-band mixer spurs as well as the fundamental leakage from the preceding frequency doubler. The signal is then boosted by a cascade of two packaged MMIC amps to generate sufficient amplitude to drive the LO port of mixer 3. The second amplifier in this chain is driven slightly into compression to reduce signal level variation over temperature.

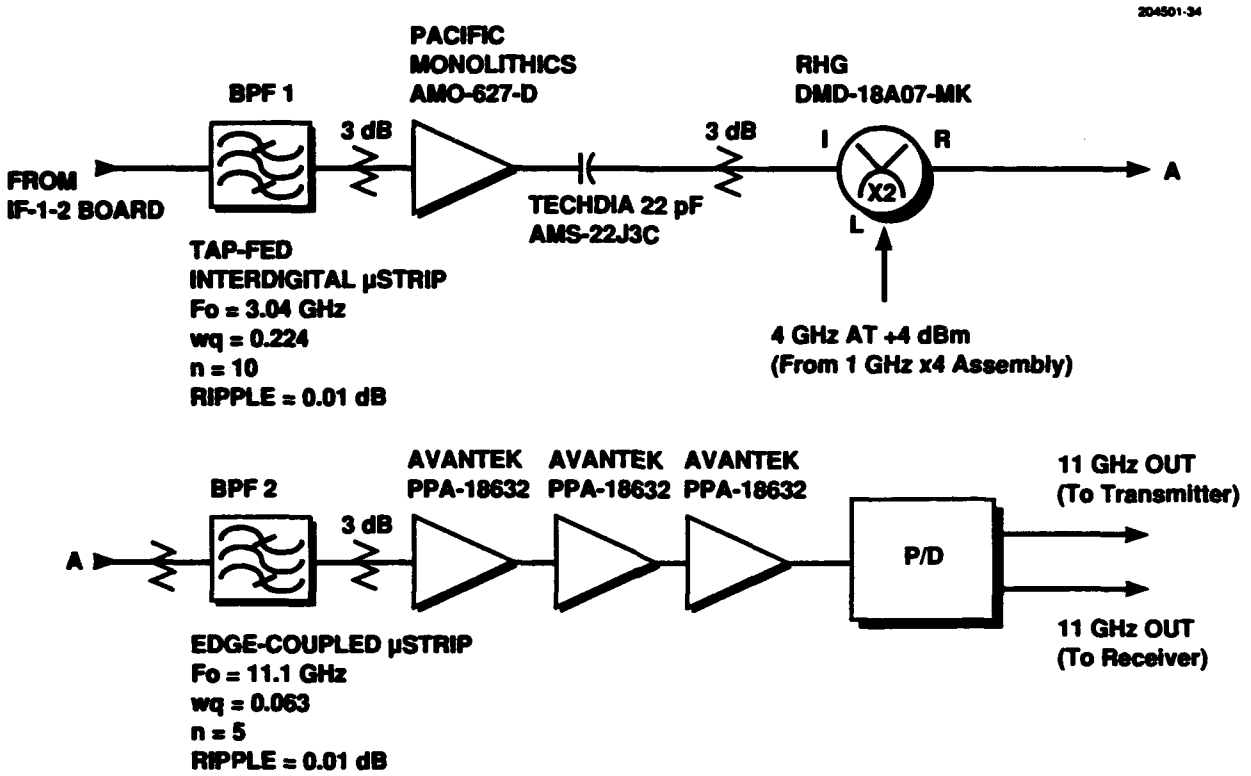
Mixer 3 is the final stage on this board, and it is the "offset mixer" that provides a sixfold expansion in the hopping tuning range that was described in Section 4.4. The mixer takes the 2.3- to 2.4-GHz band from the preceding amplifiers at its LO port and mixes it with the single selected tone from the SFB in the LO Module that arrives at its IF port. The output is a hopping bandwidth of 600 MHz between 2.8 and 3.4 GHz.

Although our PC board was designed to minimize coupling between the different sections, it became apparent during integration testing that the combination of high gain amplifiers and multiple stages of upconversion was creating additional spurious signals in the output. To eliminate this problem the inside of the module's cover was lined with a carbon-loaded, EMI gasket material and Eccosorb. This design improved the ground connection between the thin walls and cover as well as damped any radiant coupling between stages.

6.3.3 IF 3- and 11-GHz Assembly

This portion of the RF Module contains the final filtering, upconversion, and amplifier stages of the hopping signal path. The input band of 2.8 to 3.4 GHz comes from the IF-1-2 board and is frequency shifted to the RFG output band of 10.8 to 11.4 GHz. The upconverter uses a 4-GHz LO that is generated in the SRD circuit described below. The 11-GHz hopping output of the RFG is split in a power divider to provide equal amplitude signals to the transmitter and receiver. The amplifier stages in this section are biased at +9 V. A schematic of the IF 3- and 11-GHz assembly is shown in Figure 34.

Due to the high microwave frequencies in this section, adequate grounding for the circuits and transmission lines was essential. To minimize the size of the filters and be able to keep tight tolerances on line geometries, the boards in this section were fabricated on ceramic substrates and mounted on gold-plated Kovar carriers. The chassis was machined to have a smooth, flat floor over this entire section to ensure good grounding contact between the Kovar carriers and the chassis. Although the Kovar carriers add extra weight, they match the thermal expansion coefficient of the brittle ceramic substrates, which is critical to avoid cracking. An additional drawback of using ceramic substrates is that it is impractical to make the individual subassemblies larger than 1 in^2 due to the risk of breakage. This resulted in nine individual substrates in this section, in addition to the two drop-in components that were mounted directly to the chassis floor. However, ceramic was still the best alternative for this portion, considering the integration necessary between transmission lines, microstrip filters, and the components that needed to be mounted directly to the chassis metal. The ceramic substrates were routed and milled by a laser process in the hybrid assembly area, which also performed all the assembly and fabrication of the circuits for this section.



NOTES
(1) +9 V TO ALL AMPS.
(2) 0.01 μF DECOUPLING ON ALL AMPS.
(3) ALL PADS ARE EMC TECH
TS05xxG (xx = Pad Value in dB).
(4) PAD VALUES ARE NOMINAL.
ACTUAL VALUES DEPEND ON AMP GAIN.
(5) POWER DIVIDER IS A SINGLE SECTION
WILKINSON BUILT ON THIN FILM ALUMINA μSTRIP.

Figure 34. IF 3- and 11-GHz assembly schematic.

Gaps between the separate substrates were kept to less than 3 mils to minimize inductive ground and signal paths at the rf interconnects. In the 11-GHz section, the cavity width was kept to less than 500 mils to avoid resonances, and extra cover mounting screws were added to keep tight contact between the cover and side walls of the cavity. We used 0-80 screws to mount the carriers to the chassis to maximize the available space for circuitry. The 11-GHz output connectors were implemented with Wiltron 50Ω glass bead feed throughs epoxied into the chassis wall with slide-on tab contacts gap-welded to the power divider output ports. (We attempted to solder the feed throughs into the chassis wall but had limited success in evenly heating the entire chassis to the required temperature.) The external connectors are field replaceable, SMA flange mounts.

The hopping 2.8- to 3.4-GHz band from mixer 3 in the IF-1-2 board is filtered by a ten-resonator, interdigital microstrip filter [14]. This filter rejects the LO leakage, lower sideband, and other mixer spurs (Manley-Rowe products) from mixer 3. The resonator lengths were trimmed by laser during active tuning to adjust the center frequency. Open stubs were gap welded to a waffle pattern of tuning dots on the input and output lines to improve in-band matching. Iterating the mask design would probably eliminate the need for most of the laser tuning. A plot of the filter response is shown in Figure 35.

A small substrate provides the 50Ω transmission line interconnect between the 3-GHz filter and the next amplifier. A chip attenuator on this interconnect board improves the interstage matching and allows for signal level adjustment. A packaged MMIC amplifier boosts the signal level prior to it being injected into the final mixer's IF port. By having a gain stage at this point, the amount of gain required at 11 GHz was reduced. The signal level was kept low enough so as not to generate excessive spurious levels at the mixer's output. This amplifier package had flanges to allow for direct mounting to the chassis floor to improve the high-frequency ground contact. Another small substrate provides the 50Ω transmission line interconnect between the 3-GHz amplifier and mixer 4. A beam lead capacitor on this board provides the necessary ac coupling, and a chip attenuator improves the interstage matching and allows for signal level adjustment.

The final upconversion stage, mixer 4, is implemented with a custom RHG even harmonic mixer fabricated on a soft substrate circuit in a "drop-in" package. The hopping 2.8- to 3.4-GHz band is mixed with a fixed 4-GHz LO to produce an output band at the desired 10.8- to 11.4-GHz output band of the RFG. An even harmonic or subharmonically pumped mixer is designed with antiparallel diode pairs and a specially tuned balun network to cancel mixing products from the LO signal's fundamental. The mixer has excellent conversion efficiency based on the LO signal's second harmonic [8]. Using this type of mixer allowed the design of the LO drive circuit with a times-4 multiplier instead of a times-8 configuration. Due to the inevitable extra loss for higher orders of multiplication, the amount of gain required after the SRD multiplier was reduced, and a more efficient, lower frequency amplifier could be used. The RHG mixer only requires a minimum of a +5-dBm LO drive level, which also helped to reduce the required gain at 4 GHz. The drawback of this mixer was its physical geometry of 1 in^2 with a 0.25-in-thick cavity that extends beneath the top surface of the microstrip. This drove the mechanical layout and design of the entire high-frequency section of the RF Module and required extra machining to mill out a well deep enough to hold the mixer package.

The 10.8- to 11.4-GHz output band of mixer 4 is filtered by an edge-coupled microstrip, band-pass filter [15]. This filter rejects the 8- and 12-GHz harmonics from the LO leakage and out-of-band mixer spurs. A plot of the filter response is shown in Figure 36.

The final amplification of the 11-GHz hopping signal was implemented with three Avantek PPA, surface mount packaged, microwave amplifiers. The combined linear gain of these amplifiers was 45 dB; however, the final gain stage was operated into compression to reduce signal level variations over temperature. At the time of the original design, these amplifiers had the best gain performance versus power consumption and size of all available solutions. However, we found that the amplifiers had a poorly designed package and required extra effort to ensure adequate grounding to prevent oscillations.

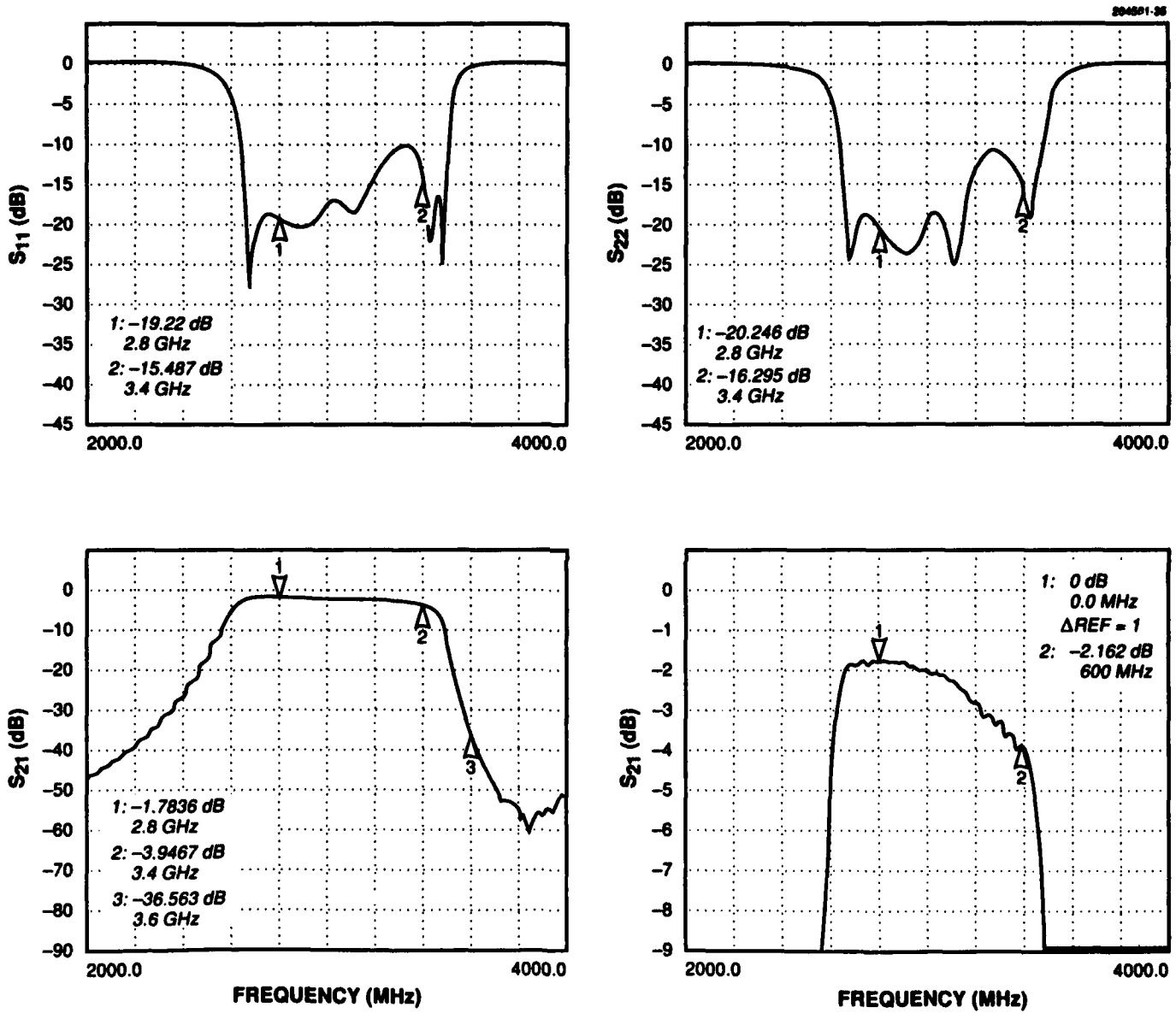


Figure 35. 3-GHz band-pass filter frequency response.

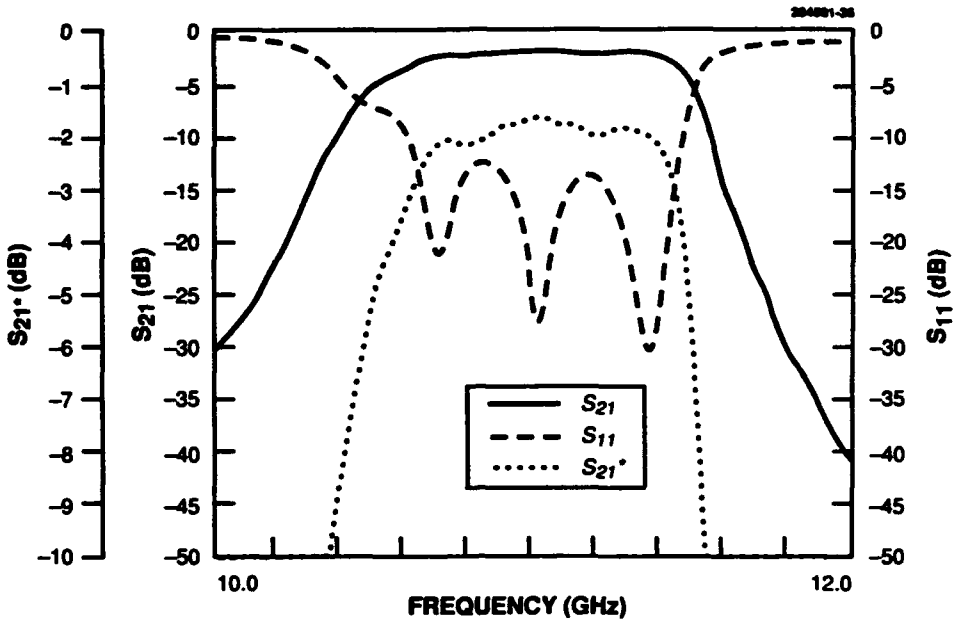


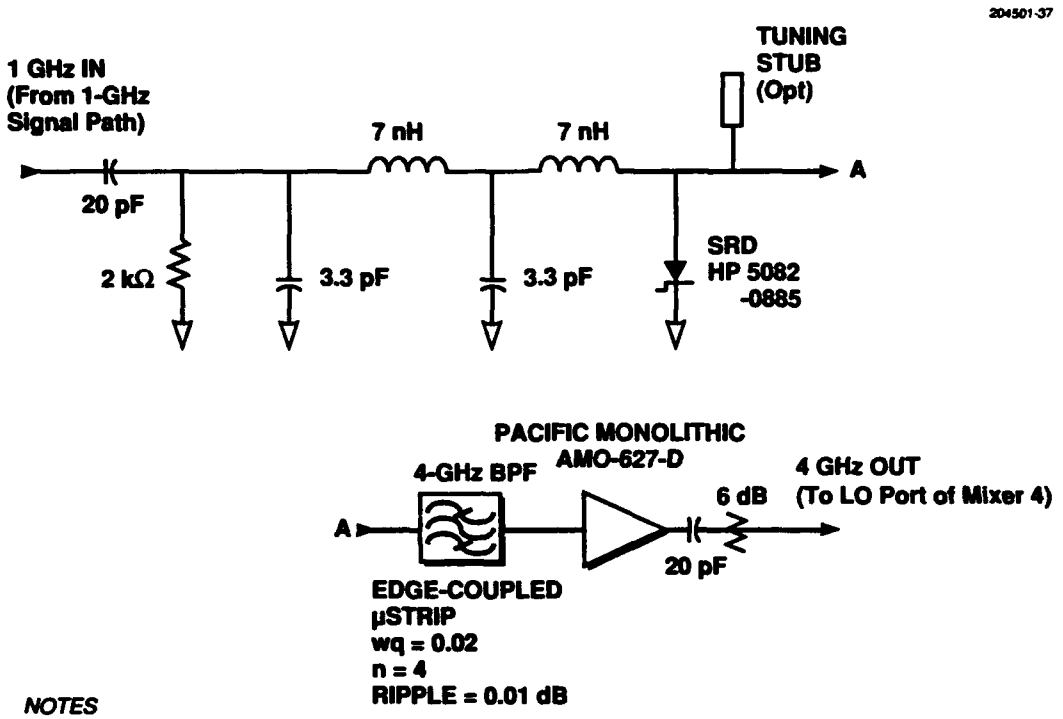
Figure 36. 11-GHz band-pass filter frequency response.

Although the manufacturer recommended mounting them to a ceramic substrate with plated through holes, we found it necessary to epoxy the package directly to a Kovar carrier. Small circular wells were milled out of the carrier directly under the amp's ports, and narrow ceramic strips brought 50Ω transmission lines to the amp's leads. This mounting configuration mimicked the test fixture that Avantek uses during their fabrication and testing. It was necessary to cover two of the amplifiers with divider walls that made electrical contact between the Kovar carrier and the module cover. This broke up the long length of the 11-GHz cavity and prevented radiant coupling between the first and last amplifier stages. To further reduce radiant coupling, the module cover was lined with Eccosorb and a conductive gasket along the cavity wall and cover interface was used. A possible replacement for this troublesome amplifier will be discussed in Section 8.

Finally, a Wilkinson power divider splits the hopping 10.8- to 11.4-GHz output to provide equal amplitude signals to the transmitter and receiver. This design was fairly straightforward and did not require any tuning. We chose a balanced output Wilkinson divider instead of an unbalanced divider or coupler because at the time of the design, the receiver had not yet been designed with its internal LO drive amplifier. The equal amplitude outputs from the RFG were designed to be sufficient to directly drive the LO port of the receiver's mixer and the transmitter's front end. Because the RFG is used in the half-duplex mode, the power divider could have been replaced with a SP2T switch to route the full signal amplitude to either the transmitter or receiver. However, we decided to keep the dual output ports. This has proven to be a very useful test point of the RFG during ASCAMP integration testing because the hopping signal from the RFG can be monitored during downlink acquisition or transmitter testing. During normal operation of the ASCAMP terminal, only the receiver or transmitter is in use at any one time, so there is no impact on performance.

6.3.4 4-GHz Multiplier Assembly

This circuitry takes the fixed frequency, 1-GHz signal from the LO Board in the LO Module and generates a 4-GHz signal used to drive the LO port of mixer 4 (described above). The fabrication technique used here was identical to that described for the IF 3- and 11-GHz assembly. A schematic of this section is shown in Figure 37.



NOTES
(1) +9 V TO AMPS.
(2) 0.01 μF DECOUPLING ON AMP.
(3) RESISTOR IS THIN FILM AND THE VALUE SHOWN IS APPROXIMATE AND REQUIRES EMPIRICAL TUNING.
(4) ALL CAPS ARE TECHDIA A-TYPE SINGLE LAYER p/n AMSxxJ2C (xx = Cap Value in pF).
(5) ALL PADS ARE EMC TECH TS05xxG (xx = Pad Value in dB).
(6) PAD VALUES ARE NOMINAL. ACTUAL VALUES DEPEND ON AMP GAIN.
(7) ALL INDUCTORS ARE BOND WIRES AND THEIR VALUES ARE APPROXIMATE AND REQUIRE EMPIRICAL TUNING.

Figure 37. 4-GHz multiplier assembly schematic.

An SRD multiplier [16,17] was used as the best and simplest alternative to perform this function. The SRD multiplier was passively biased to help prevent oscillations and was tuned for a single frequency output at 4 GHz. The input matching network for the SRD was a two-section, low-pass filter topology. The series inductors were implemented with thin gold wires bonded in a matrix network to a waffle pattern of tuning dots. (Tuning of the SRD to maximize output power was accomplished by removing some of the bond wires in order to vary the inductance.) An open stub was gap welded to a waffle pattern of tuning dots on the input line to improve in-band matching. An open stub was gap welded to a waffle pattern of tuning dots on the output line of the SRD to improve interstage matching with the band-pass filter.

The edge coupled microstrip band-pass filter [15] was incorporated into the SRD's output circuit and was integrated with the SRD during tuning. This filter rejects the undesired harmonics from the multiplier. The harmonics reflected back into the SRD regenerate to improve signal level at the desired 4-GHz output. A plot of the filter response is shown in Figure 38.

The 4-GHz output was then boosted by a packaged MMIC amplifier that was operated in compression to minimize signal level variations over temperature. The output of the amplifier was sent through a chip attenuator to improve interstage matching with the LO port of mixer 4 and to set the power level. The 4-GHz multiplier assembly was tested on a fixture over temperature, input dynamic range, and over frequency (outside its nominal 1-GHz fixed input frequency) to assure that this circuit was completely stable. This assembly was by far the most tuning intensive circuit of the entire RFG. If there had been a suitable alternative, we would have used it.

6.3.5 9-V Regulator

A simple linear regulator was used to produce the +9-V bias required by the Pacific Monolithic and Avantek microwave amplifiers used in the high-frequency sections. A simple circuit was implemented to allow the regulator to be turned on via a TTL control. (An alternative resistor-capacitor time constant circuit was designed to allow the regulator to automatically turn on slowly, but this was rejected because it was inconvenient to use during terminal integration testing.) This circuit was intended to prevent excess current drain on the dc converter system during the ASCAMP terminal power-on sequence. A schematic is shown in Figure 39.

6.4 PACKAGING DESIGN DETAILS

The RFG comprises three separate chassis that can be fabricated, assembled, and tested independently. Figure 40 shows the RFG in two pieces with the covers removed. Figure 41 shows the interior of the TMXO and LO Module. Figure 42 shows the interior of the RF Module. Figure 43 shows RFG completely assembled, and Figure 44 is a picture of the RFG mounted into the ASCAMP terminal electronics enclosure.

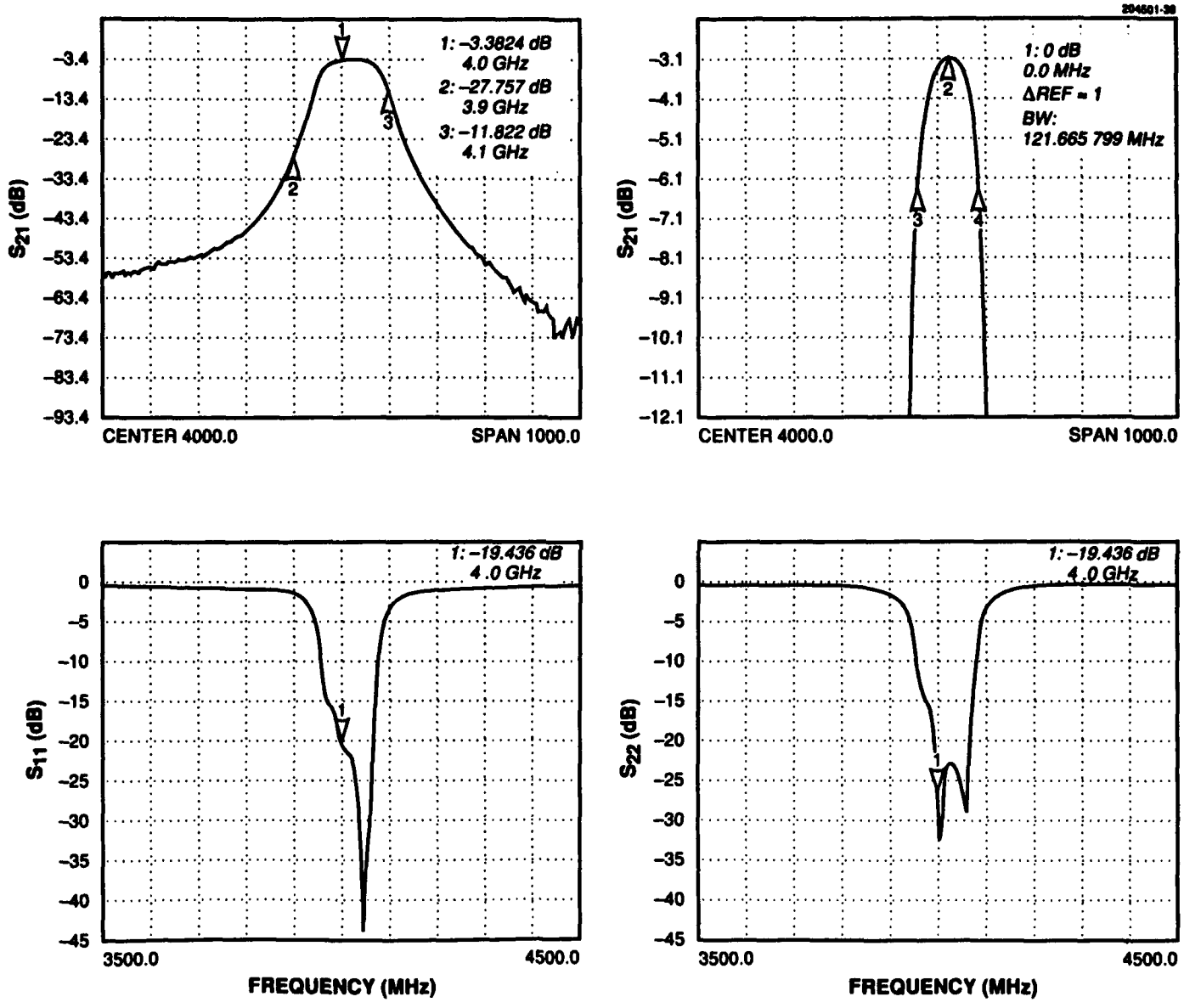


Figure 38. 4-GHz band-pass filter frequency response.

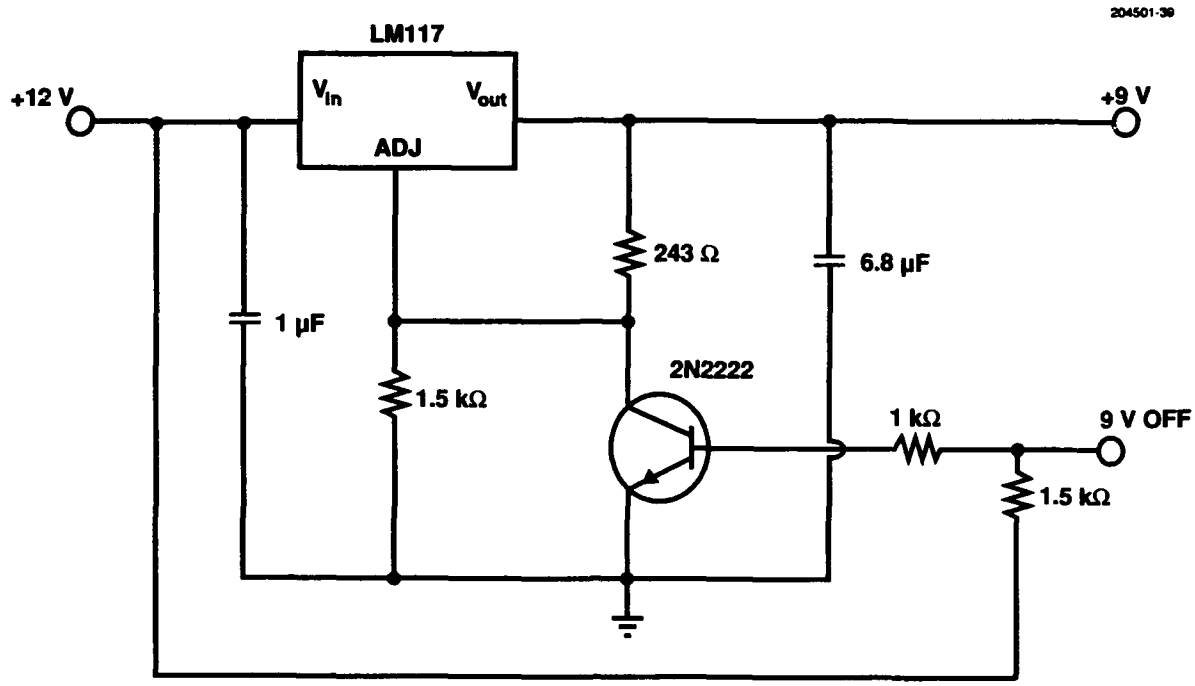


Figure 39. +9-V regulator schematic.

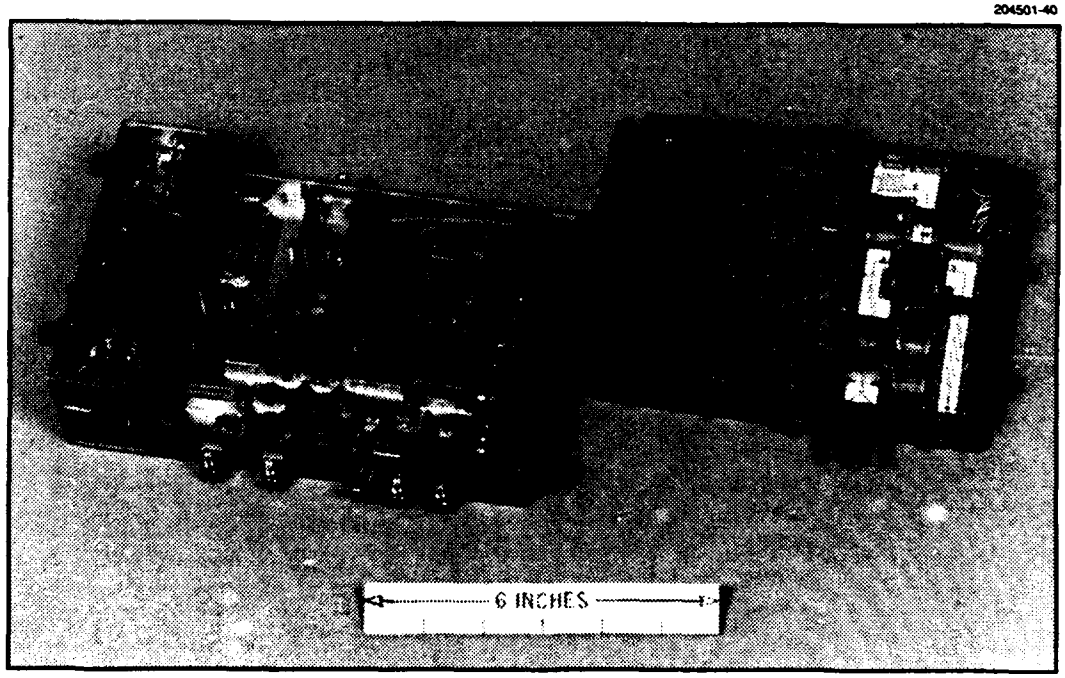


Figure 40. RF Generator partially disass bled.

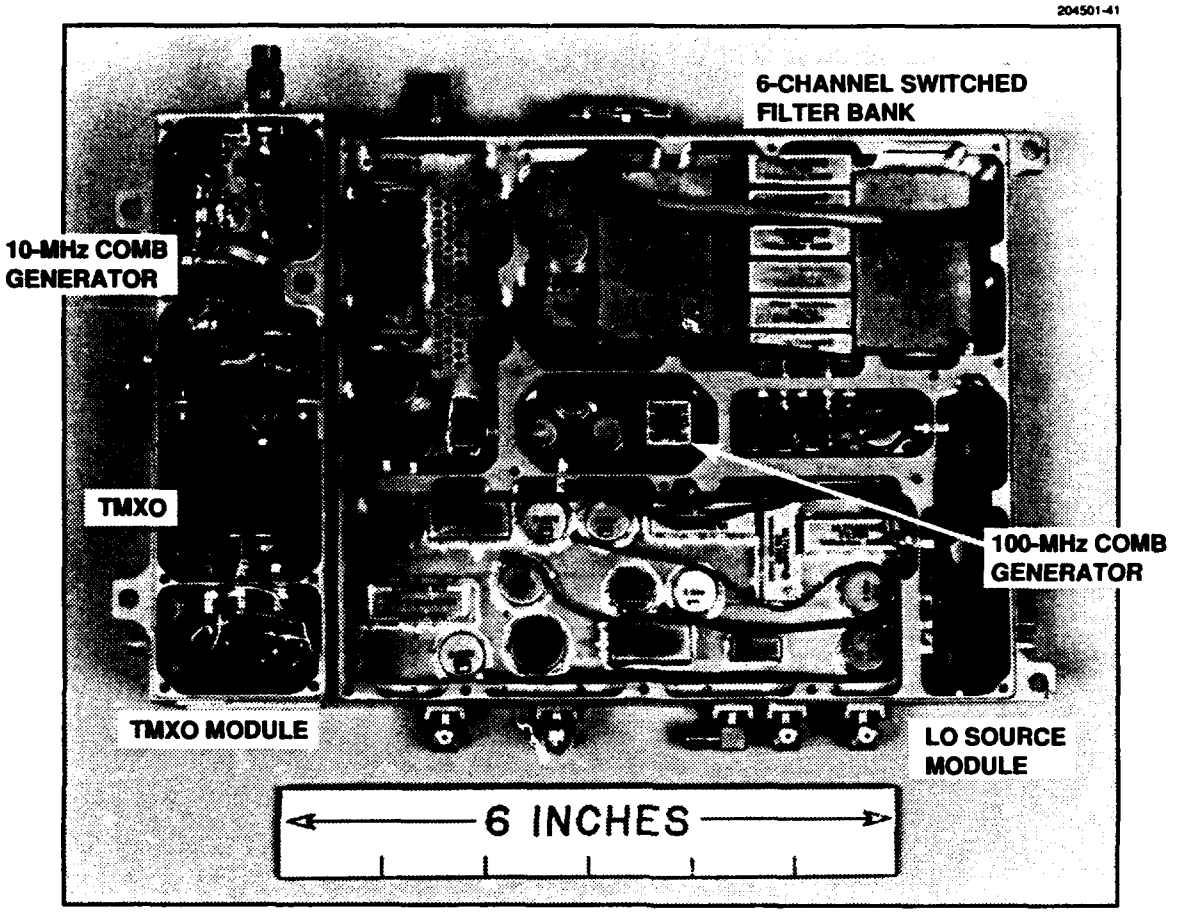


Figure 41. TMXO and LO Modules with covers removed.

The mechanical design had a priority of keeping weight to a minimum. The chassis were machined from aluminum blocks with numerically controlled milling machines. The chassis are hollow frames with internal divider walls to separate the different circuitry sections. The PC cards are mounted to small bosses. For the higher frequency boards, where grounding was critical (including the SFB, LO Board, and the IF-1-2 board), the bosses were extended to thin ledges that extend around the perimeter of the boards. The high-frequency section in the RF Module, which contains the 4-GHz multiplier and the IF 3- and 11-GHz assembly, was fabricated to have a flat floor to provide adequate grounding for the circuits built with ceramic substrates and Kovar carriers. That floor thickness was made as thin as possible to save weight but thick enough to support the tapped holes used to mount the carriers.

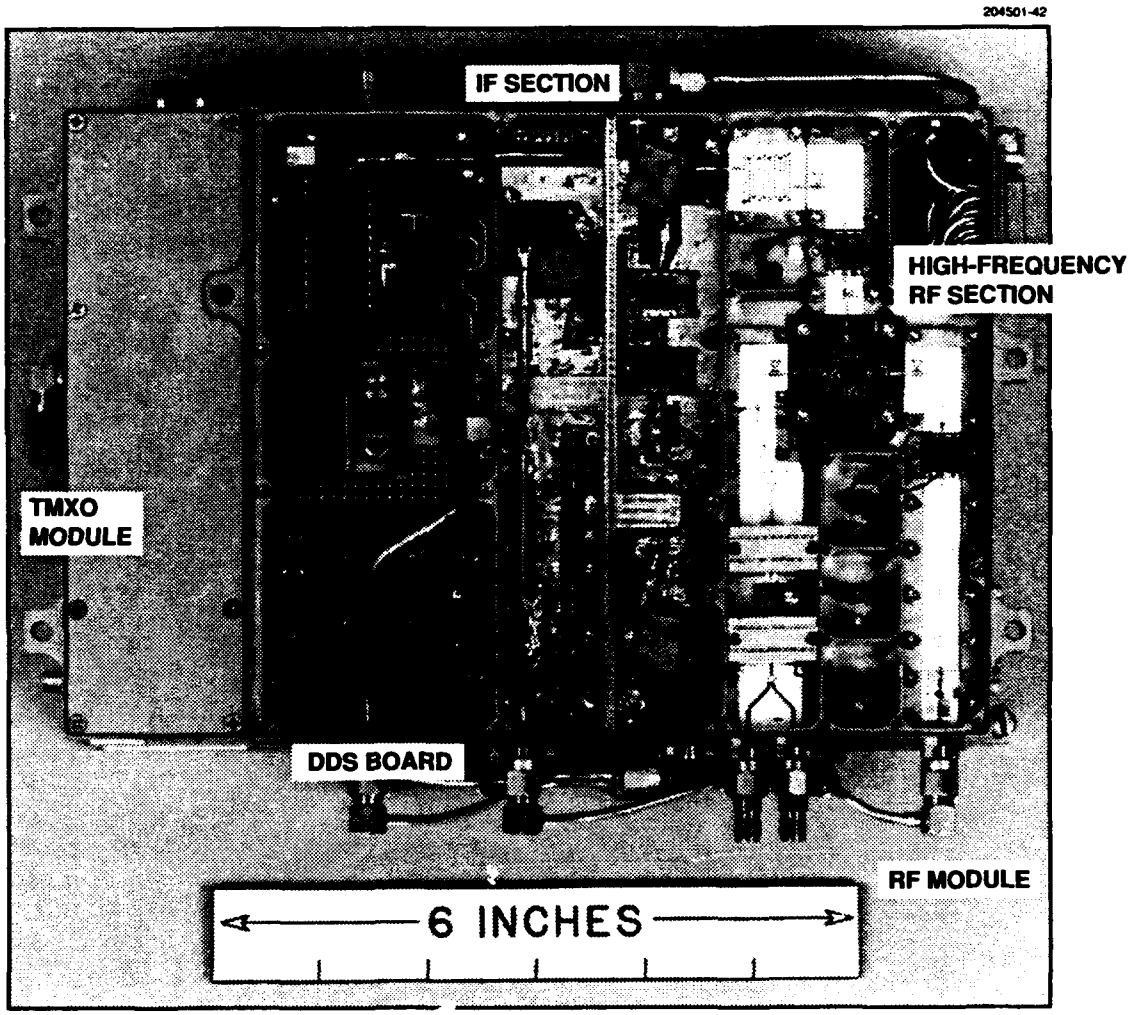


Figure 42. RF Module with cover removed.

The outer walls were machined to a 0.070-in thickness. The typical thickness of the internal walls and covers was kept to 0.030 in, except for mounting points and thermal paths. Mounting bosses in the interior walls that support the cover were undercut to remove excess metal.

Extra thickness was designed into one wall of the RF Module to provide a good thermal path for a component on the DDS board. The STEL NCO dissipates approximately 7 W of dc power and has a maximum case temperature of +125°C. The NCO has 2-56 studs that protrude from the top of the package that are designed as a heatsink mounting point. A specially designed, gold-plated, copper heatsink was mounted to the top of the NCO with thermal RTV. The heatsink was made from two thick copper plates that were soldered to 5-mil stress relief shims bent to 90°. The mounting holes in the heatsink were

machined slots, and locknuts were set so that the connection was not torqued tight. The combination of the flexible, thermal RTV and lockscrews allowed for mechanical stress relief. The other mounting surface of the heatsink was tightly attached to the adjacent wall of the RFG chassis. That wall was machined to a 0.125-in thickness to improve thermal transfer. A mounting foot of the RFG is located less than 1 in from this heatsink to provide a low-resistance thermal path to the ASCAMP center web. Extensive thermal testing was conducted to ensure that the temperature rise of the NCO did not exceed allowable limits. This testing was conducted with the RFG mounted to the ASCAMP chassis with thermal loads simulating the digital stack in place. The DAC on the DDS board had a finned heatsink attached to it with thermal RTV. The purpose of this heatsink was to facilitate radiant thermal transfer to the module cover. This heatsink was sufficient to cool the DAC whose maximum junction and maximum operating temperatures are +175°C and +140°C, respectively. Table 16 shows the measured temperature of various test points of the RFG after it had been operating at ambient for 3.5 h. (The PPA amplifiers in the table are the 11-GHz output amps.) Figure 45 shows the thermal rise of various test points over time, while the RFG was being operated at ambient with a thermal load simulating the digital stack.

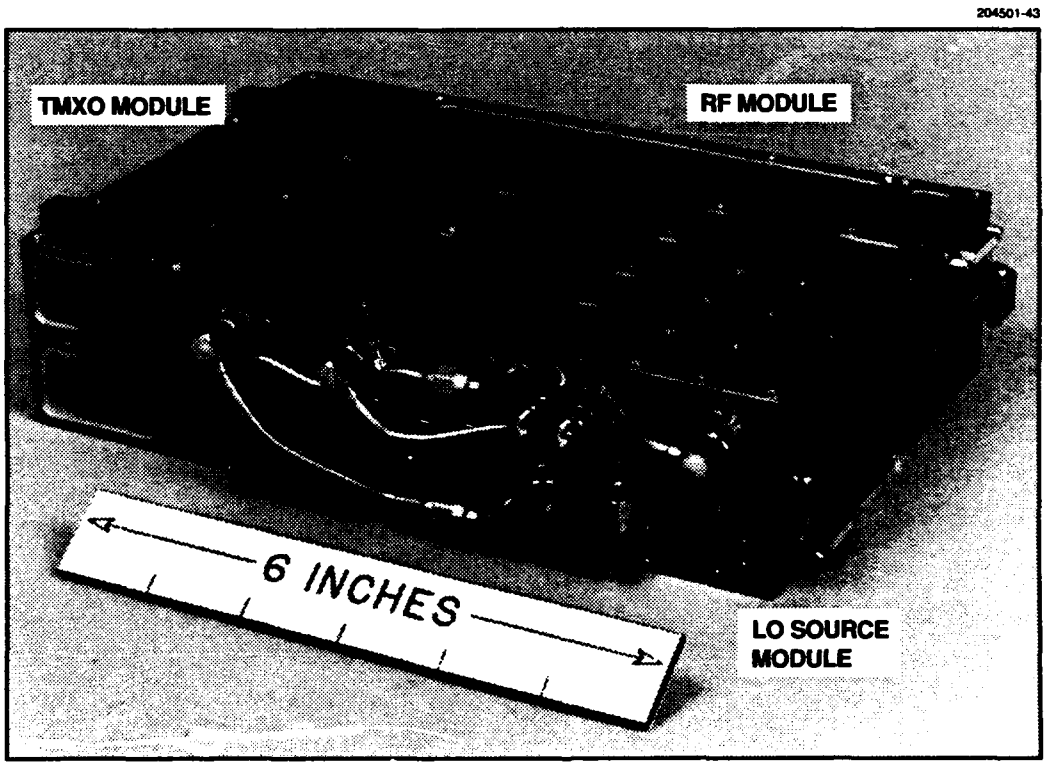


Figure 43. RF Generator completely assembled.

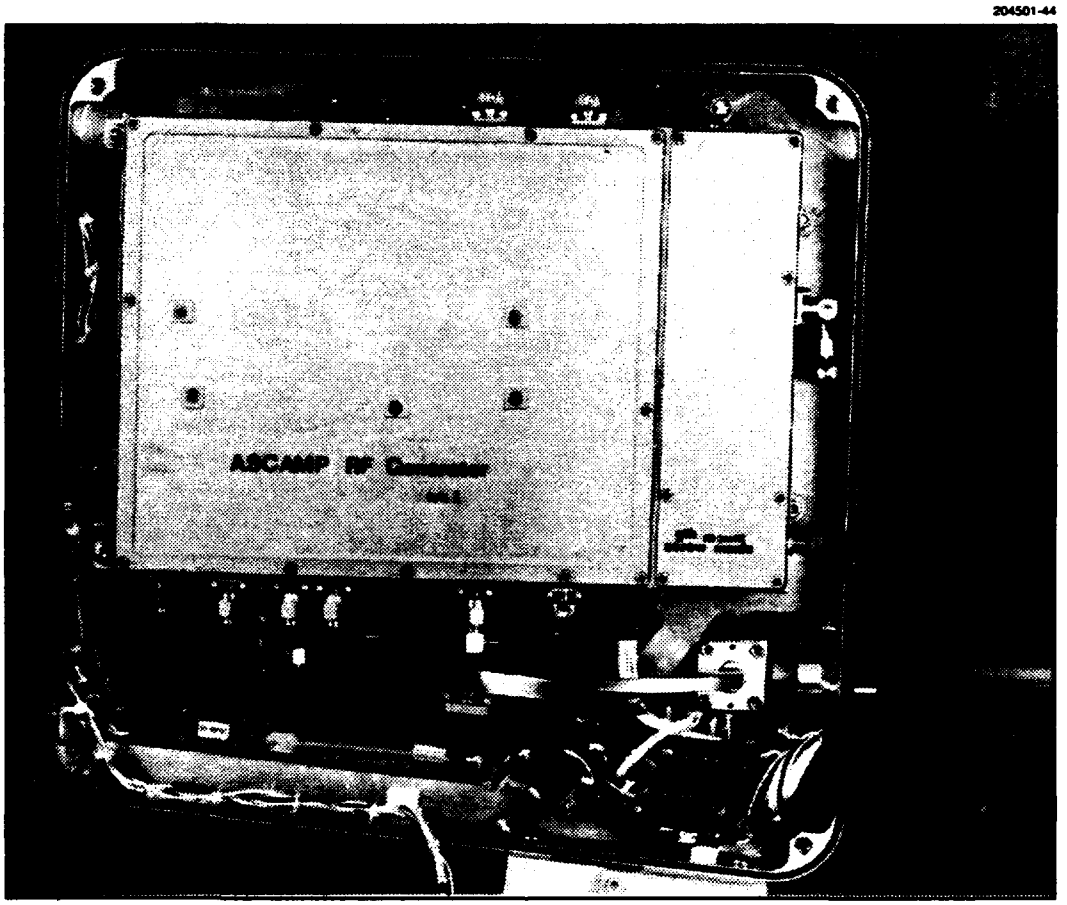


Figure 44. RF Generator mounting configuration.

Table 17 shows the weight of the chassis and covers. Also, the total assembled weight of the modules is provided, which includes PC boards, components, and mounting hardware. The packing density is a ratio of the weight of the circuitry and components to the chassis weight. It is a measure of how dense the circuitry is inside an electronic enclosure. The packing densities of the modules in the RFG are very high and indicate the lightness of the structure and the dense package design. (Note that the higher weight of the RF Module is due to the heavy Kovar carriers in the high-frequency circuits.)

Because the chassis was fabricated from aluminum, some protection was required to prevent oxidation. The 11-GHz connectors in the RF Module required glass bead feed throughs to be soldered or epoxied to the chassis wall; therefore, the chassis needed to be copper plated to allow for solder or epoxy adhesion. To ensure proper operation, low-inductance interconnects, and good grounding in the high-frequency circuits in the RF Module, the Kovar carriers were gold plated. To prevent deterioration between dissimilar metals, the entire RF Module was gold plated. Copper- and gold-plating of the TMXO and LO Modules was considered optional, although it allowed for superior, low-inductance ground paths that can be critical to synthesizer designs where there are high isolation requirements.

TABLE 16

Measured Operating Temperature of RF Generator

Test Point	Temperature (°C)
NCO heatsink	55.5
NCO thermal path	42.3
DAC w/o heatsink	73.5
DAC w/heatsink	60.4
PPA amplifier	46.7
RF Module cover	34.0
Ambient	23.1

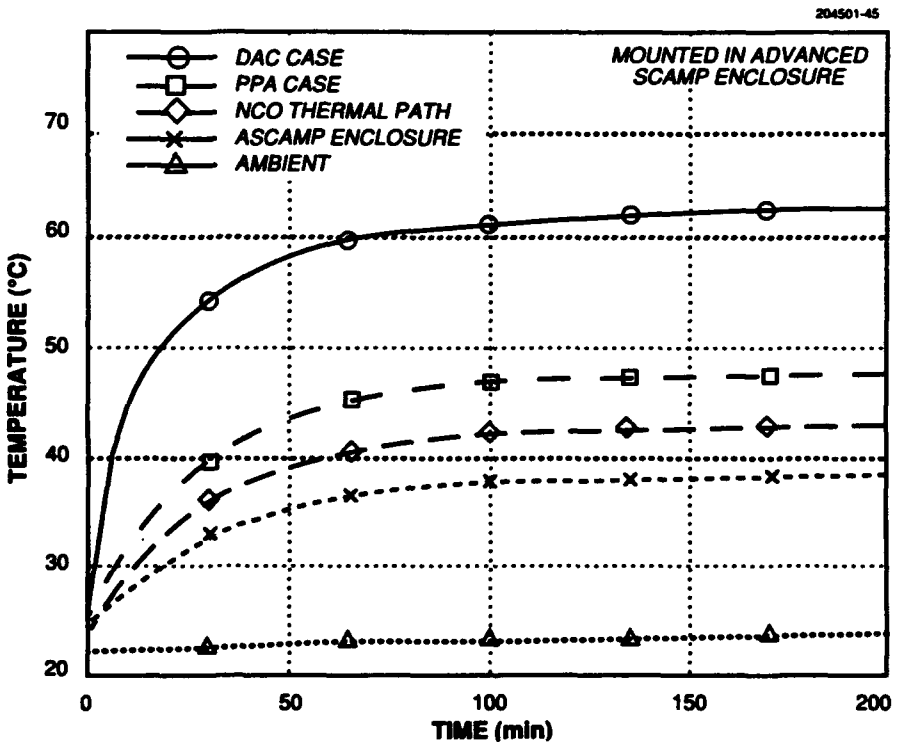


Figure 45. RF Generator thermal rise

TABLE 17

RF Generator Weight Details

	Chassis (lbs)	Cover (lbs)	Complete with Circuits (lbs)	Packing Density (%)
TMXO Module	0.16	0.08	0.53	54.7
RF Module	0.44	0.26	1.62	56.8
LO Module	0.43	0.26	1.25	44.8
RF Generator Total	1.03	0.60	3.40	52.1

7. PERFORMANCE RESULTS

Two RFGs, developed and built at Lincoln Laboratory, have been delivered for integration into ASCAMP terminals. This section summarizes the data that has been taken on these units.

The RFG was designed to meet the system requirements of the ASCAMP terminal as it was conceived in 1989/1990. The critical performance goals of the RFG include output power over frequency and temperature, frequency tuning resolution and speed, and noise due to spurious and phase noise. Size, weight, and dc power are also critical to all systems in the portable ASCAMP terminal, and these parameters are summarized in Table 18.

TABLE 18

Physical Parameter Summary

Size	Weight	dc Power
90 in^3	3.4 lb	17.5 W

A more detailed look at the individual dc power consumptions of the individual boards is shown in Table 19.

7.1 OUTPUT POWER VERSUS FREQUENCY

The 10.8- to 11.4-GHz output of the RFG drives the LO port of the receiver front end as well as the pre-amp in the transmitter front end. It is essential that the output signal level from the RFG be relatively constant over temperature and frequency to minimize variation in performance of the receiver and transmitter. The output power of RFG s/n 2 is plotted in Figure 46 (10 dB per division) and Figure 47 (1 dB per division) and shows the output power versus its tuning range over a range of temperature from –30°C to +60°C. The data indicate that the typical variation in output power at any one temperature is ±1.0 dB and that the worst-case variation over frequency and temperature is ±1.6 dB. This variation is well within the original goals of 4-dB peak-to-peak, which was determined from the input dynamic range of the receiver and transmitter. Integration measurements with the receiver and transmitter were conducted; they showed that this variation caused no perceptible degradation to system performance.

7.2 FREQUENCY HOPPING: SWITCHING SPEED AND RESOLUTION

As an agile synthesizer in a frequency hopping system, the RFG must be capable of tuning to a specific frequency very quickly, and once at the new frequency, its output phase must settle within a small fraction of a hop period. Inability to tune quickly would result in a decrease in uplink and downlink signal strength, while phase changes during the hop degrade the DPSK demodulator performance.

TABLE 19

Board Level Power Consumption

Board	+5-V Bias (mA)	–5-V Bias (mA)	+12-V Bias (mA)*	Total Power (W)
TMXO			13	0.156
10-MHz comb generator			29	0.348
100-MHz reference	53			0.265
100-MHz comb generator	179	72		1.255
Coupler board	15			0.075
LO Board	243			1.215
Switched filter board	16			0.080
DDS	32	1906		9.69
IF-1-2 board	57		92	1.389
4-GHz SRD			53	0.636
IF 3- and 11-GHz assembly			198	2.376
Total RFG	595	1978	385	17.485

* Note that circuits listed in this column use a linear regulator to drop their actual bias voltage to either +5 or +9 V.

The classic technique for determining the frequency settling time of a synthesizer is to directly measure the output phase while hopping between two known frequencies. This is accomplished by mixing, or "beating," the output down to 0 Hz. A fixed frequency synthesizer, tuned to the same frequency as one of the hopping frequencies, is used as an LO source in a mixer/phase detector. This test method gives a direct measure of the amplitude and duration of any phase transients associated with hopping. Unfortunately, this method requires not only being able to phase lock a reference source to the output of a hopping synthesizer but also ensuring that the phase difference between the two are in quadrature. For the ASCAMP RFG, this task is nearly impossible for most output frequencies due to the nature of the DDS and the random "roll-over" in its accumulator while hopping. The measurement data

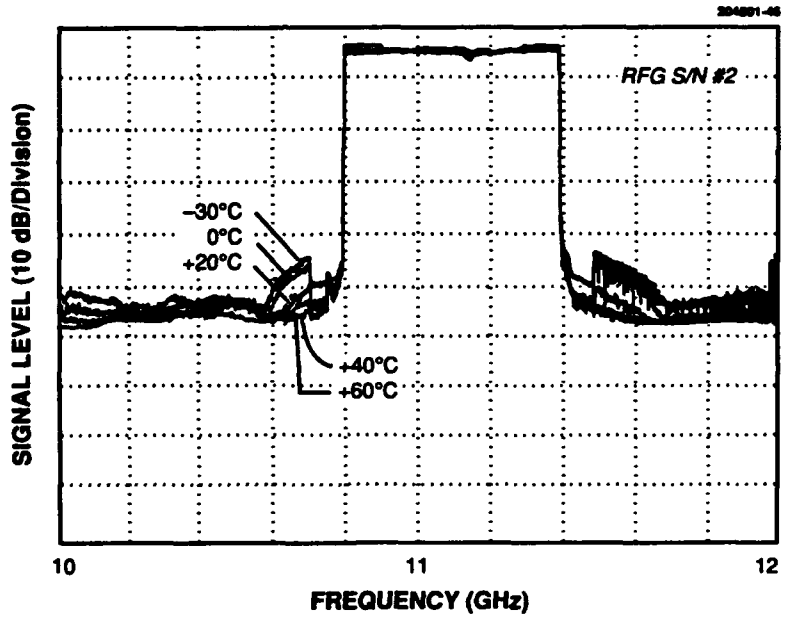


Figure 46. Output power over frequency and temperature (10 dB/division).

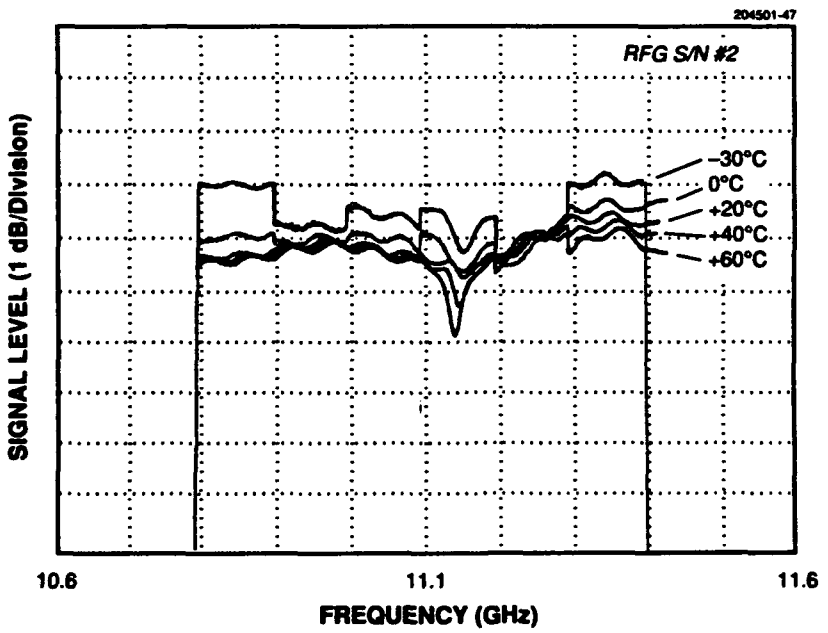
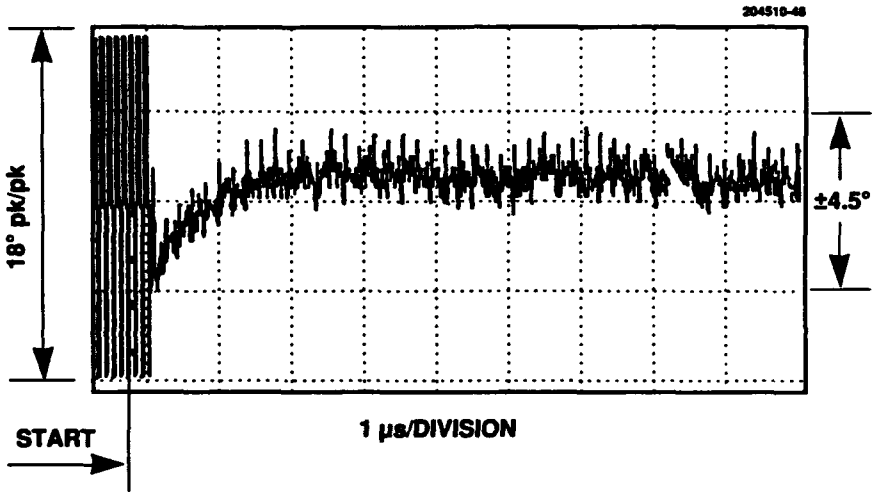


Figure 47. Output power over frequency and temperature (1 dB/division.)

presented here were obtained by measuring phase transients for many hops but only recording the data when the RFG and reference source were in quadrature (as indicated by very small phase difference after settling). Figure 48 is a typical plot of the phase transient of the RFG. It shows the phase settling transient as the RFG hops from 11.09 to 11.05 GHz. The graph indicates that the RFG has hopped to the exact frequency and settled within 500 ns (where settling is defined when the phase is within ±4.5 deg of its final phase).

As a side effect of measuring settling time, this technique also provides verification of the frequency accuracy and resolution of the RFG. In order for the phase detector to measure zero phase error, the synthesizer under test must be at exactly the same frequency as the test equipment, which has a tuning resolution of approximately 2 Hz.



RFG FREQUENCY SETTLING TIME

	f_a	f_b
RFG_{OUT}	11.09 GHz	11.05 GHz
DDS_{OUT}	95.0 MHz	75.0 MHz
DDS_{HEX}	25111112	24000000

- DETECT PHASE ON f_a
- DDS SWITCHED
- SFB FIXED (700 MHz)

Figure 48. Frequency hopping and phase settling measurement.

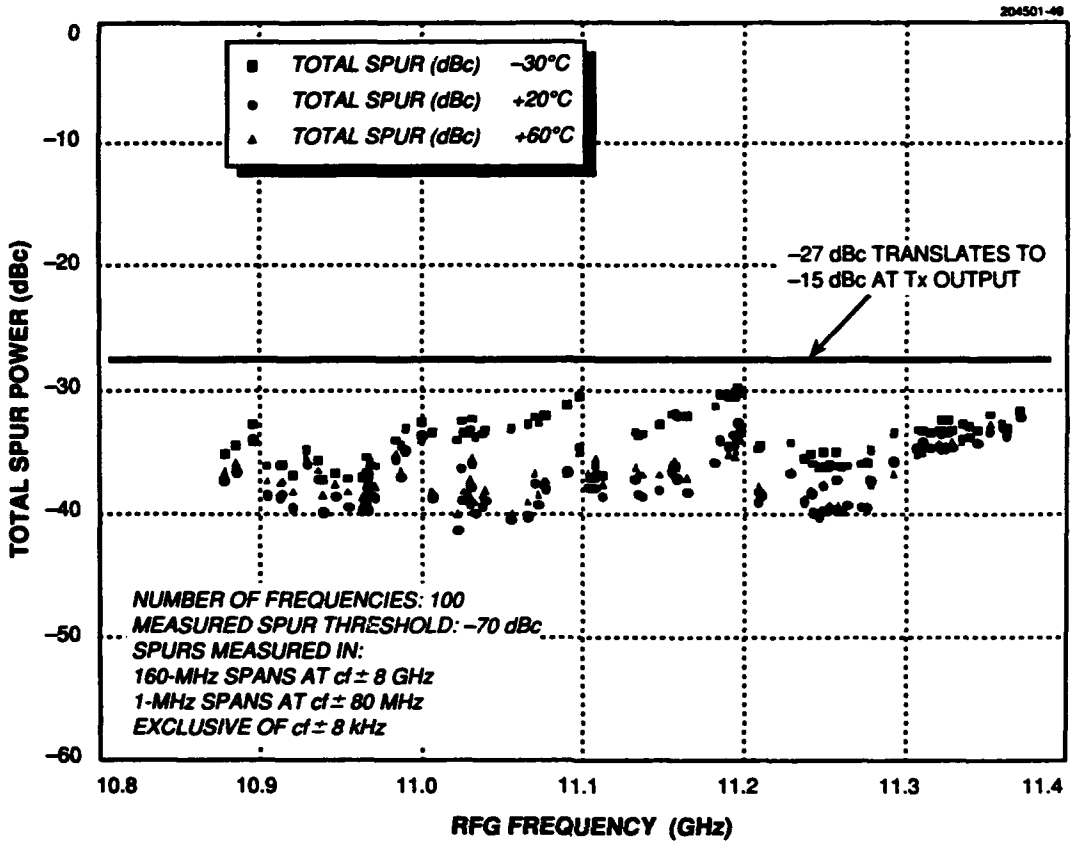
7.3 SPURIOUS PERFORMANCE

The spurious performance of the RFG was calculated by adding the total spur power at each output frequency. This method is significantly different from the way synthesizer spurious performance is usually presented. The more common methods are to measure a *single* worst-case spur at a single synthesizer tuning frequency or sometimes the average spur level at a *single* output frequency. These techniques provide an overly optimistic measure of how a synthesizer can affect system performance, especially for designs that incorporate a DDS that has spurious components spread over a wide frequency band. A more accurate technique is to measure the energy of *all* of the spurs that accompany a given synthesizer output frequency. The measurement bandwidth will vary depending on the system level performance criteria under consideration. In other words, if one is concerned about carrier suppression, then the power contained in all of the spurs within the transmitter's bandwidth must be added to yield a single total spur power for each output frequency in the synthesizer's tuning range. If one is concerned with interchannel interference, then the power contained in all spurs that are offset from the carrier within the channel bandwidth must be added to yield a total channel bandwidth spur power for each frequency in the synthesizer's tuning range.

In the EHF spread spectrum system, it is impractical to measure spurious performance at all of the possible output frequencies due to the sheer magnitude of valid tuning frequencies. However, it is possible to measure all of the spurious signals, above a reasonable threshold, for every tuned frequency in a given set. For our measurements, two sets of pseudorandom frequencies were generated: one set of 100 frequencies and another set of 1000 frequencies. Due to the extensive time required to make the spur measurement on the set of 1000 frequencies (over 120 h), measurements were made with this set only once. These data were used to verify the statistical validity of data taken on the smaller set of 100 frequencies. All of the data presented here were taken with the 100 frequency set. Figure 49 is a plot of the total spur power at each of the 100 output frequencies across the RFG output tuning range. Note that each data point represents the total energy from all spurs within ±8 GHz of the carrier; this measurement bandwidth is significantly more conservative than measuring only within the transmitter's input bandwidth. Figure 50 is a plot of the total energy from all spurs contained within the worst-case, sliding 10-MHz window found within 20 MHz of the carrier. These data are used to quantify the amount of interchannel interference.

To provide a more realistic representation of the system performance, measurements were taken at the transmitter's output when it was being driven by the RFG. Figure 51 is a plot of the total spur power measured within 2 GHz of the carrier. Figure 52 is a plot of total energy from all spurs contained within the worst-case, sliding 10-MHz window found within 20 MHz of the carrier.

The data summarized in Table 20 indicate that the RFG will provide acceptable spurious performance in the ASCAMP terminal. Note that this table lists the mean of the total spur power across the output frequency band.

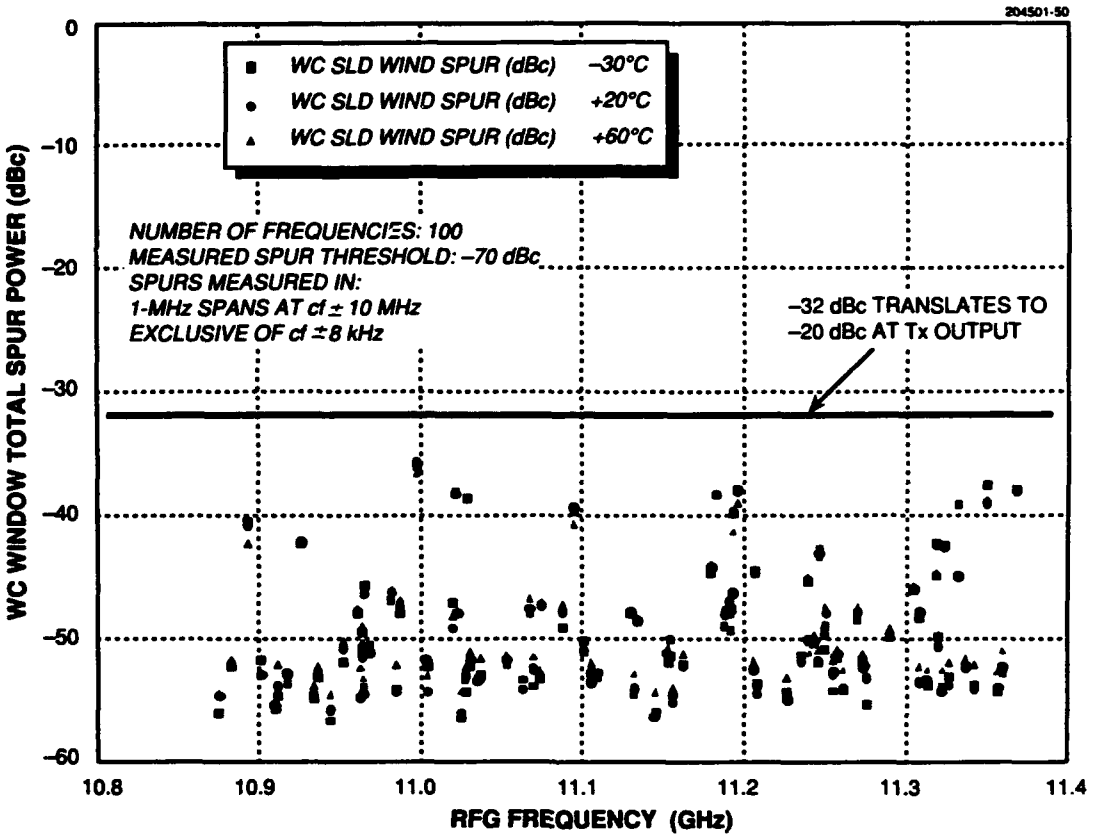


	–30°C	+20°C	+60°C
MINIMUM	–37.37	–41.40	–40.10
MAXIMUM	–29.81	–32.30	–32.00
MEAN	–34.02	–37.21	–36.75
STD DEVIATION	1.94	2.28	1.98
VARIANCE	3.76	5.21	3.93

Figure 49. RF Generator total spur power.

7.4 PHASE NOISE

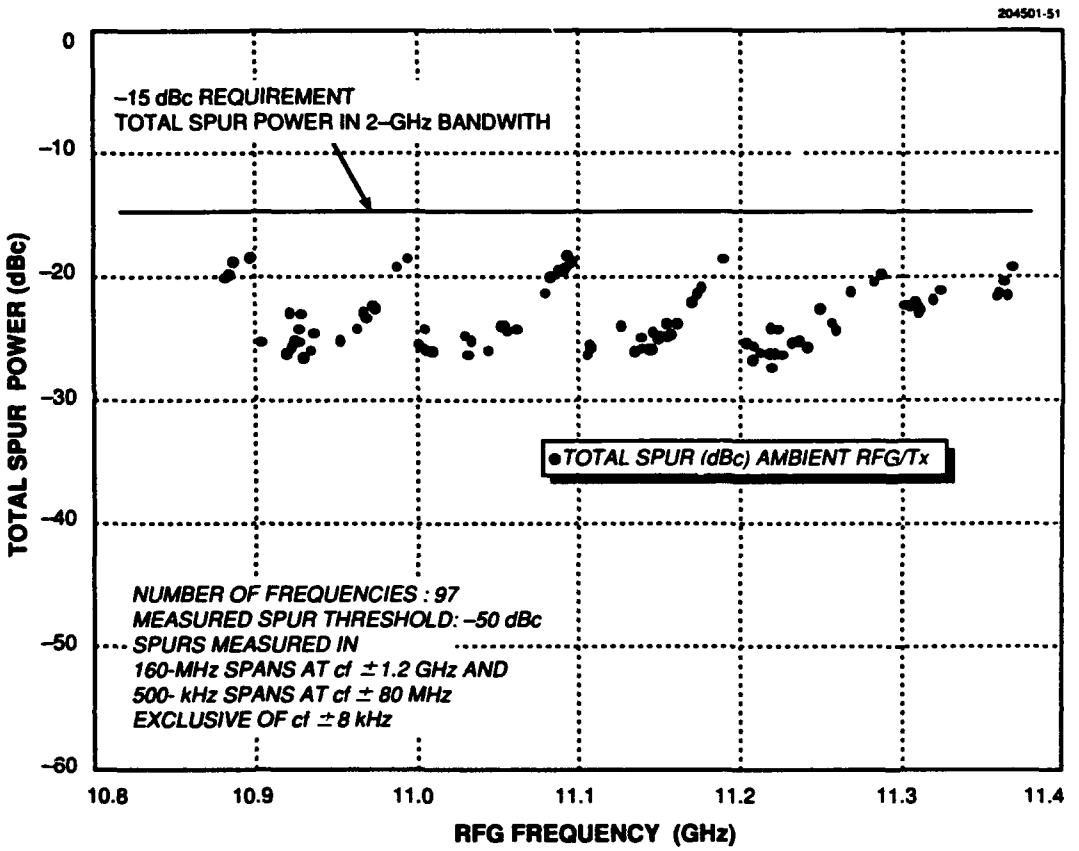
The RFG phase noise is dominated by the internal 1-GHz fixed frequency source which, after frequency multiplication, is used as an LO signal for the final upconversion stage. Excessive phase noise in the RFG can cause carrier suppression in the output signal of the transmitter, which directly degrades the link margin. The RFG's goal was to have the sum of all broadband noise, both phase and spurious, cause less than 0.1 dB of the transmitter carrier suppression. Phase noise and spurious also affect system



	–30°C	+20°C	+60°C
MINIMUM	–56.59	–56.26	–55.76
MAXIMUM	–36.00	–35.57	–36.54
MEAN	–49.61	–49.52	–49.00
STD DEVIATION	5.14	5.00	4.51
VARIANCE	26.42	25.02	20.33

Figure 50. RF Generator total spur power in worst-case sliding 10-MHz window.

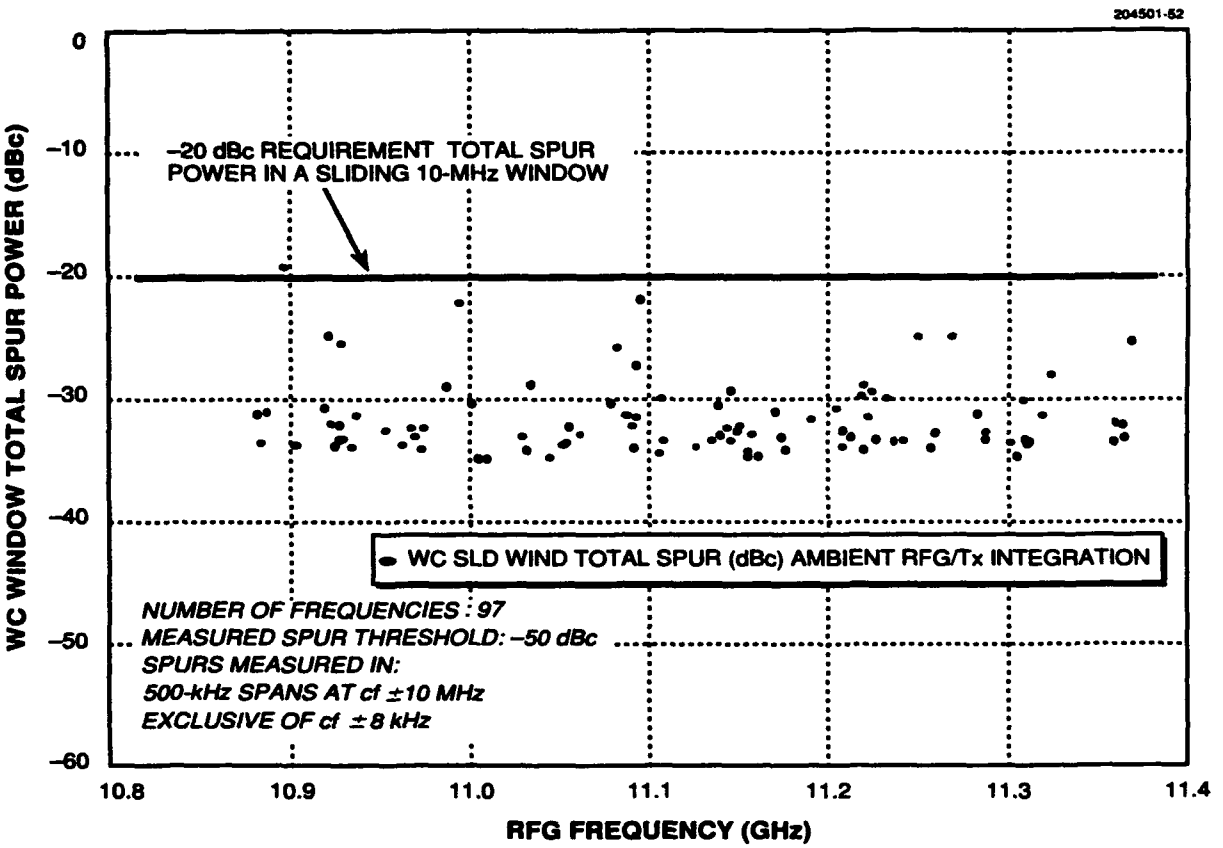
level parameters such as interchannel interference. (Note that carrier suppression related noise measurements integrate the total noise over the full spectrum, whereas interference-related noise measurements integrate the total noise over only limited bandwidths.) The phase noise of the RFG can be measured directly with a spectrum analyzer. A plot of the phase noise is shown in Figure 53.



	RFG/Tx AMBIENT
MINIMUM	-27.25
MAXIMUM	-18.22
MEAN	-23.31
STD DEVIATION	2.48
VARIANCE	6.14

NOTE: X-AXIS IS RFG OUTPUT FREQUENCY, BUT DATA WAS TAKEN AT TRANSMITTER OUTPUT (44 GHz)

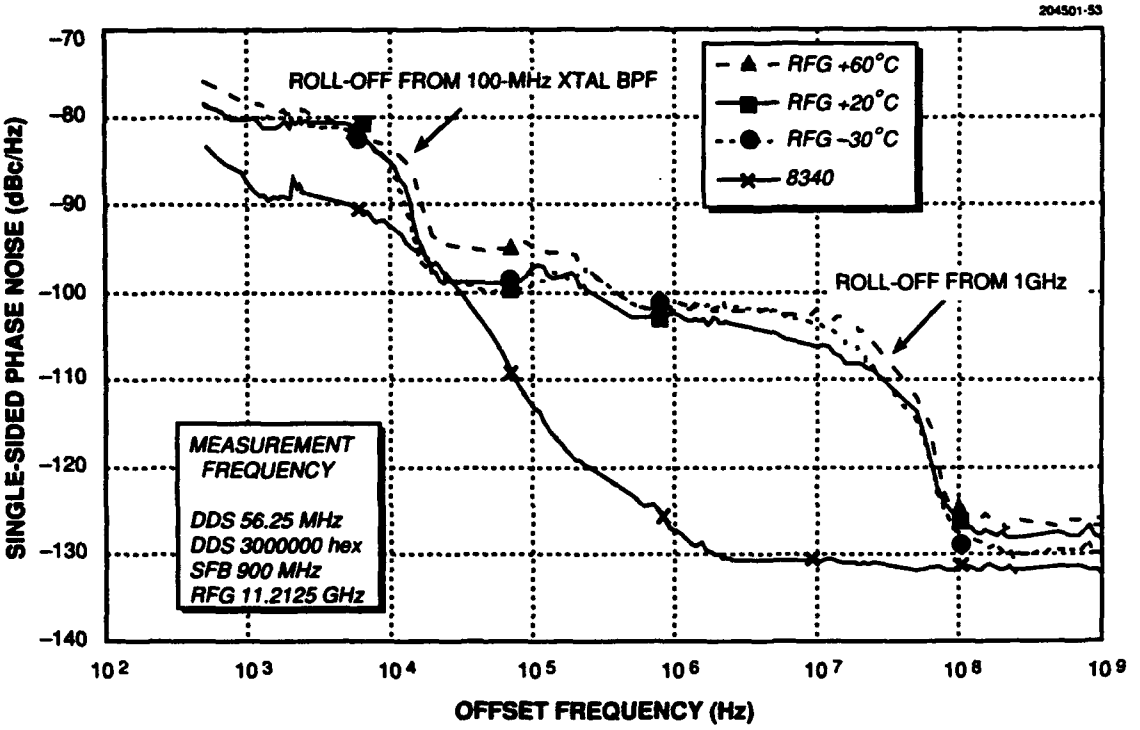
Figure 51. RF Generator/Transmitter integration: total spur power.



	RFG/Tx AMBIENT
MINIMUM	–34.84
MAXIMUM	–19.23 **
MEAN	–31.65
STD DEVIATION	3.06
VARIANCE	9.39

NOTE: X-AXIS IS RFG OUTPUT FREQUENCY, BUT DATA WAS TAKEN AT Tx OUTPUT (44 GHz).

Figure 52. RF Generator/Transmitter integration: total spur power in worst-case sliding 10-MHz window.



MEASUREMENT	TOTAL CNR (2S) 500 Hz TO 1 GHz (dBc)	PARTIAL CNR ±5 MHz, excl ±8 kHz (dBc)
RFG +60° C	-23.86	-30.93
RFG +20°C	-26.57	-32.83
RFG -30°C	-25.56	-31.34
HP 8340 (ref)	-37.65	-47.04

Figure 53. RF Generator phase noise at 11-GHz output.

TABLE 20

RF Generator Noise Measurement Summary

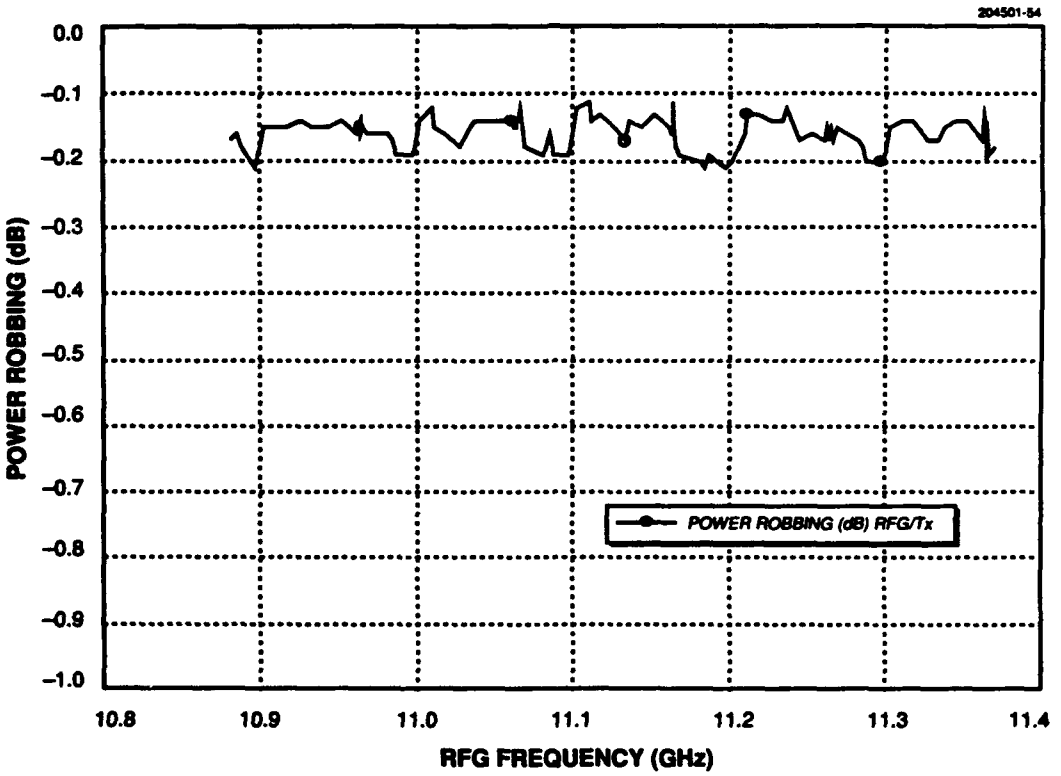
Temp °C	Mean Spurious		Phase Noise		Total Noise	
	Broadband dBc	10 MHz dBc	Broadband dBc	10 MHz dBc	Broadband dBc	10 MHz dBc
+60	–36.8	–49.0	–23.9	–30.9	–23.7	–30.8
+20	–37.2	–49.5	–26.6	–32.8	–26.2	–32.7
–30	–34.0	–49.6	–25.6	–31.3	–25.0	–31.2

7.5 NOISE SUMMARY

Table 20 summarizes the spurious and phase noise measurements that have been previously discussed. Note individual entries for phase noise and spurious power as well as combinations of both. The data are broken out into broadband (carrier suppression) and limited bandwidth (interchannel interference) measurements. The phase noise pedestal, at offsets between 20 kHz and 20 MHz from the carrier, dominates the integrated noise level. (A technique for improving the phase noise is described in the Section 8.)

7.6 CARRIER SUPPRESSION AND POWER ROBBING

To get a more direct measure of how noise in the RFG (both phase and spurious) will suppress the output carrier of the transmitter, "power robbing" tests were conducted. In this test, the output power of the transmitter was measured in a very narrow bandwidth while it was being driven by the RFG. Then, a clean, bench-top synthesizer was substituted for the RFG, and the transmitter output power was measured again. The difference between these two power measurements is the amount by which the transmitter carrier has been suppressed by noise in the RFG. A plot of the power robbing, or carrier suppression, is shown in Figure 54. As can be seen from the graph, the RFG causes an average of 0.16-dB carrier suppression due to its noise.



MEASUREMENT	MEAN	STD DEVIATION	VARIANCE
RFG/Tx	-0.16	0.023	0.0005

Figure 54. RF Generator/Transmitter integration: carrier suppression.

8. RECOMMENDATIONS FOR FUTURE IMPROVEMENTS

Two classes of improvements could be made to the current RFG design: incremental and evolutionary. Incremental modifications could be made to the current design to improve performance, while evolutionary changes would require a complete redesign based on knowledge gained from this project.

8.1 INCREMENTAL IMPROVEMENTS

A few modifications could be made within the framework of the current design to improve performance, namely, reducing phase noise and lowering dc power consumption. Some of these modifications are being incorporated into the third RFG that is currently being built.

Two circuits that can easily be replaced to reduce power consumption are the 100-MHz comb generator in the LO Module and the 11-GHz amplifiers in the final stage of the RF Module. Motorola has recently developed a new, fast logic family called ECLipse. Although the internal gate propagation delays are slightly slower than GaAs, it is fast enough for our application. A comb generator built with an ECLipse, quad NOR gate was tested, and its output harmonics are comparable to those with the GBL device in the current RFG. Figure 55 is a plot of the output spectrum of an ECLipse comb generator followed by a low-power buffer amp, which makes the output levels equivalent to the GBL design. The total bias for the board, including the amplifier, is +5 V at 52 mA = 0.26 W. This is a savings of almost 1 W compared to the GBL design in the current RFG. A new two-sided FR4 PC board has been fabricated that is a drop-in replacement for the six-layer board required for the original design.

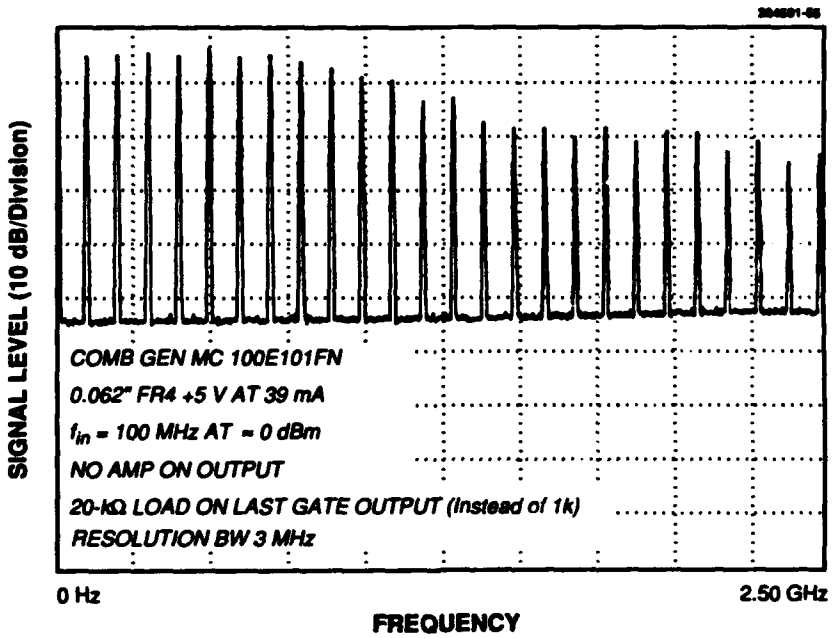


Figure 55. Motorola ECLipse comb generator spectral output.

Another recent development has been new, low-power amplifiers from Sierra Microwave that are built in a very small form factor. We have procured custom amps that were designed to meet our requirements. They have comparable gain and output power to the Avantek PPA amps currently being used, but they only require a bias of +5 V at 165 mA = 0.825 W. This is a savings of over 0.8 W compared to the Avantek amps in the current RFG. The Sierra amps have been measured to verify performance, and they are being incorporated into the s/n 3 RFG. Figure 56 is a plot of the compression curve of the Sierra amp, and Figure 57 is a plot of the linear gain frequency response. A very important side benefit of these new amplifiers is the inherent improvement in produceability and reliability due to the better design and packaging of these amps over the Avantek design.

Another incremental improvement that can be made to the current RFG is a reduction of phase noise that would directly lead to an improvement in total noise power. As discussed in Section 5.4.2, the plateau of noise at offsets from the carrier between 1 and 20 MHz is a major contributor to the total phase noise of the RFG. By replacing the 1-GHz band-pass filter with one designed with a narrower noise

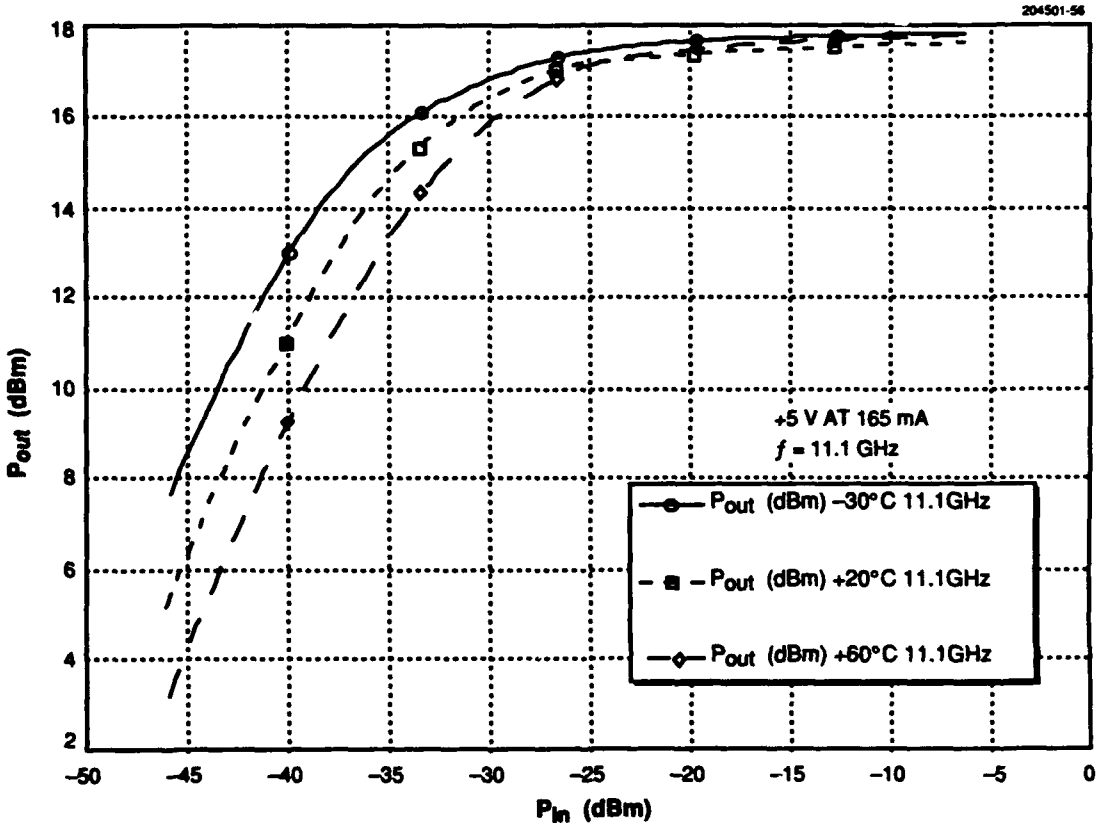


Figure 56. 11-GHz Sierra microwave amplifier compression curve.

bandwidth, the plateau can be made to roll-off at a lower frequency and reduce the total integrated noise. A custom, two-section filter designed with high-Q helical resonators was procured from Anthony RF. It is slightly larger than the current filter but was able to fit in the LO Board with minor rework of the mounting holes. This filter has a 3-dB bandwidth of 8 MHz compared to the currently used filter that has a 65-MHz bandwidth. As seen in phase noise model in Figure 58, this improvement should yield a total phase noise for the RFG of –32 dBc, which is a 6-dB reduction from the current design. This modification is being incorporated into the s/n 3 RFG.

Other alternatives to improving the phase noise include replacement of the 4-GHz edge-coupled filter with a dielectric resonator or another high-Q filter design. This would also help reduce the noise bandwidth of the RFG and lower the total noise power. A PLL could be used as a replacement for the 4-GHz SRD multiplier; however, a PLL would lead to an added, unnecessary complexity in the fabrication and alignment procedure of the RFG and might cause problems with any active power control implementation.

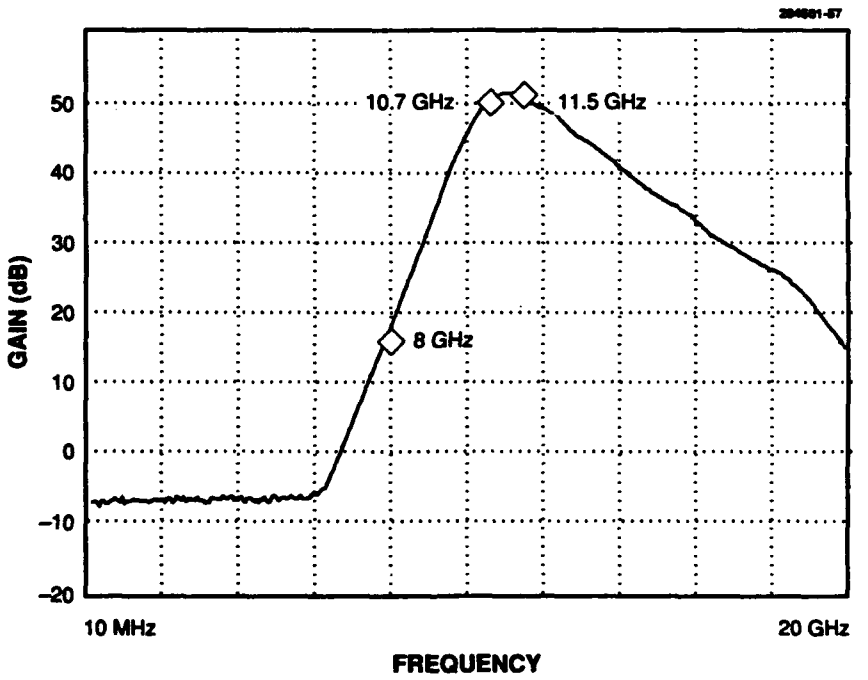
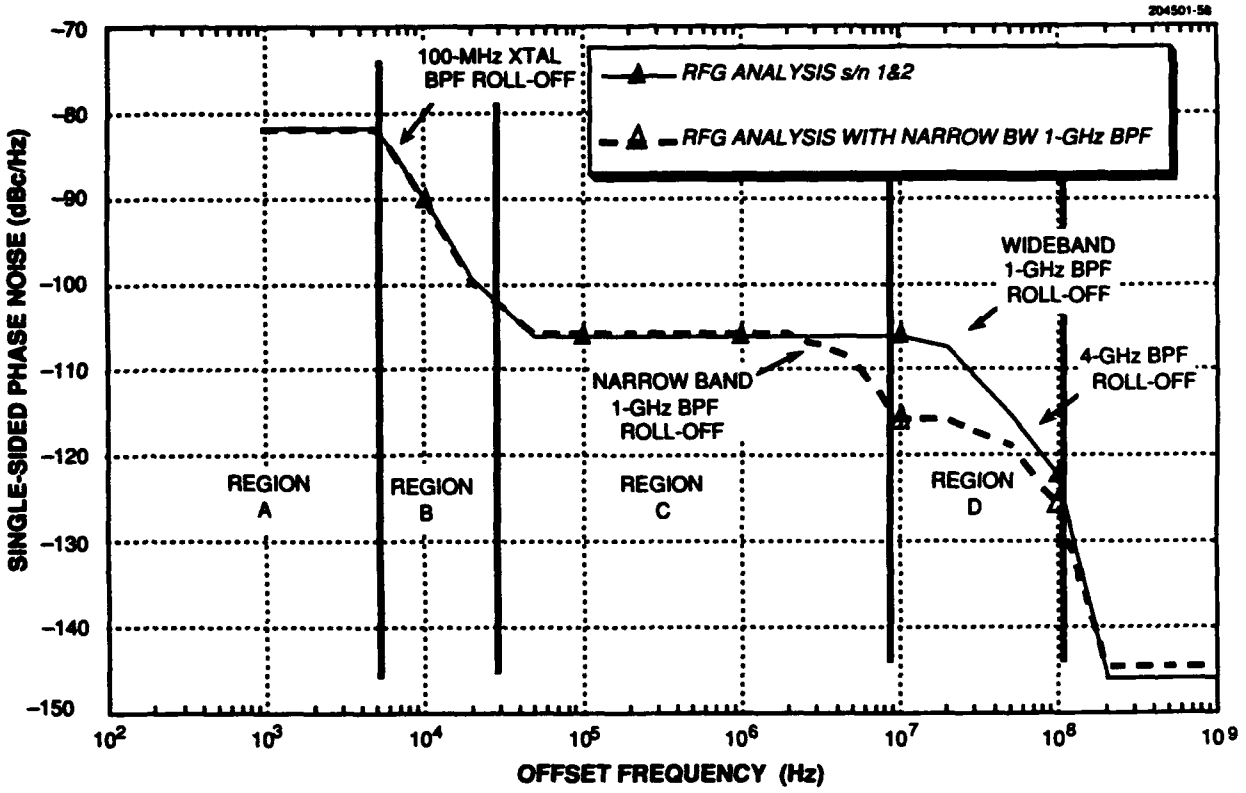


Figure 57. 11-GHz Sierra microwave amplifier frequency response.



MEASUREMENT	TOTAL CNR (2S) 1 kHz TO 1 GHz (dBc)	PARTIAL CNR ±5 MHz, EXCL ± 8 kHz (dBc)
RFG W/ WIDE 1-GHz BPF	-27.25	-35.76
RFG W/ NARROW 1-GHz BPF	-31.69	-36.21

Figure 58. Comparative phase noise with narrow band 1-GHz filter.

8.2 EVOLUTIONARY IMPROVEMENTS

One of the most important changes that could be incorporated into a next-generation RFG is to use a new DDS. The current DDS board consumes 55% of the total dc power of the RFG and only produces 8% of the required bandwidth. Taking advantage of new developments in DDS technology could lead to substantial reduction in dc power and increase the available bandwidth from the DDS, thereby reducing the amount of additional circuitry required. As an example, Plessey has recently started delivering its GaAs DDS that has a usable bandwidth in excess of 200 MHz but requires only 5 W of dc power.

One of the lessons learned during the development of the ASCAMP RFG was that the size of the filters was a limiting factor in trying to reduce the overall volume. Also, the number of upconversion stages in the hopping signal path directly increased the complexity and difficulty in minimizing spurious. An improved frequency plan would reduce the number of mixers between the DDS and the 11-GHz output and reduce the total number of required filters (perhaps at the expense of more stringent filter designs). This improvement would lead to reduced size, better spurious, and easier alignment and testing.

In conjunction with reducing the number of mixer stages, a future design should reduce the number of compressed amplifiers in the hopping rf signal path. Compressed amplifiers can degrade the frequency settling times due to the time constants in their bias networks. Minimizing the number of amplifiers that are in compression would increase the settling time margin.

Another way to reduce size would be to incorporate more MMIC amplifiers. Over the last few years, MMIC gain stages have become more readily available. They could replace the hybrid amplifiers in TO-8 cans that are currently used in the RFG in circuits less than 3 GHz. The drawback of the early MMIC designs was that they required more dc power than the hybrid counterparts. The MMIC designs have been improved recently, and their dc power requirements are now comparable, or only slightly higher, than hybrids for many applications.

More complex MMIC designs that incorporate a higher level of integration (e.g., upconverter stages with gain) are still not commercially available at low cost. However, they could be procured through a development contract with a foundry that included nonrecurring engineering funding. This type of MMIC would be able to significantly reduce the size of a next-generation RFG.

Another aspect of the RFG design that could be improved is the packaging. The current design of many independent circuits facilitated the development cycle. However, a higher level of integration of circuit functionality on fewer PC boards would reduce manufacturing cost and improve produceability. Care would need to be taken to provide sufficient isolation between the sensitive circuits so as not to degrade noise and spurious performance.

9. CONCLUSIONS

A frequency generator system has been described that was designed using a novel mixture of direct digital and direct analog synthesizer techniques. The size and performance of this synthesizer makes it well suited for the class of man-portable EHF terminals like the ASCAMP being developed at Lincoln Laboratory. This methodology of synthesizer design is quickly becoming more accepted in the communications community, and many other systems now incorporate similar architectures.

Two RF Generators were designed, developed, and built at Lincoln Laboratory. The RF Generators have been successfully integrated with available subsystems of the ASCAMP terminals, including the receiver, transmitter, Keystream Processor and dc converter. All of the data that has been taken, including the results of integration tests, indicate that the RFG will provide adequate and acceptable performance for the ASCAMP terminal.

Numerous lessons have been learned that will lead to improvements in the next-generation synthesizer designs as well as ways to retrofit the current RF Generators to yield performance enhancements.

GLOSSARY

A	Amperes
ASCAMP	Advanced Single Channel Anti-Jam Man-Portable
ASIC	Application Specific Integrated Circuit
BPF	Band-Pass Filter
BW	Bandwidth
CMOS	Complementary Metal Oxide Silicon
DAC	Digital-to-Analog Converter
dB	decibels
dBc	decibels relative to carrier
dBm	decibel-milliwatts
dc	Direct Current; or Data Clock
DDS	Direct Digital Synthesizer
DPSK	Differential Phase Shift Keying
ECL	Emitter Coupled Logic
EHF	Extremely High Frequency
EMI	Electro-Magnetic Interference
EMXO	Efratom Miniaturized Crystal Oscillator
FET	Field Effect Transistor
FSK	Frequency Shift Keying
GaAs	Gallium Arsenide
GBL	Giga-Bit Logic
GHz	1,000,000,000 Hertz
Hz	Hertz
IB	In-Band
IC	Integrated Circuit
IF	Intermediate Frequency
kHz	1,000 Hertz
KP	Keystream Processor
LO	Local Oscillator
mA	milliamperes
MHz	1,000,000 Hertz
MIC	Microwave Integrated Circuit
MILSTAR	Military and Strategic Tactical Relay
MMIC	Monolithic Microwave Integrated Circuit

NCO	Numerically Controlled Oscillator
PC	Printed Circuit Board
PLL	Phase Lock Loop
RF	Radio Frequency
RFG	RF Generator
ROM	Read Only Memory
SAW	Surface Acoustic Wave
SCAMP	Single Channel Anti-Jam Man-Portable
SCOTT	Single Channel Objective Tactical Terminal
SFB	Switched Filter Bank
SMA	(a type of coaxial rf connector)
SP6T	Single Pole, Six Throw
SPST	Single Pole, Single Throw
SRD	Step Recovery Diode
STel	Stanford Telecommunications
TMXO	Tactical Miniaturized Crystal Oscillator
TTL	Transistor-Transistor Logic
UHF	Ultra-High Frequency
V	Volts
VCO	Voltage Controlled Oscillator
W	Watts

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13. ABSTRACT (*Maximum 200 words*)

This report describes a combination agile synthesizer and reference frequency generator called the RF Generator, which was developed for use in the Advanced SCAMP (ASCAMP) program. The ASCAMP is a hand-carried, battery-powered, man-portable ground terminal that is being developed for EHF satellite communications. In order to successfully achieve a truly portable terminal, all of the subsystems and components in ASCAMP were designed with the following critical goals: low power, lightweight, and small size.

The RF Generator is based on a hybrid design approach of direct digital and direct analog synthesis techniques that was optimized for small size, low power consumption, fast tuning, low spurious, and low phase noise.

The RF Generator was conceived with the philosophy that simplicity of design would lead to a synthesizer that differentiates itself from those used in the past by its ease of fabrication and tuning. By avoiding more complex design approaches, namely, indirect analog (phase lock loops), a more easily produceable design could be achieved. An effort was made to minimize the amount of circuitry in the RF Generator, thereby making trade-offs in performance versus complexity and parts count when it was appropriate.

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